Service Guide

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For Safety information, Warranties, and Regulatory information, see the pages at the end of the book.

Agilent Technologies 16600A-Series Logic Analysis System

Agilent 16600A-Series Logic Analysis System

The Agilent Technologies 16600A-series are 100 MHz state, 500 MHz timing logic analysis systems. The 16600A-series also provide one slot for an emulation module and one slot for other measurement modules.

Features

Some of the main features of the 16600A-series are as follows:

- 204 data channels in the 16600A
  136 data channels in the 16601A
  102 data channels in the 16602A
  68 data channels in the 16603A
- 64 MByte RAM (160 MByte optional)
- 4.3-Gbyte hard disk drive
- High-density 3.5-inch flexible disk drive
- Keyboard
- Mouse interface
- Intermodule triggering and time correlation of acquired data
- RS-232-C or Centronics interfaces for hardcopy output to a printer or RS-232-C or LAN controller interface
- Target Control

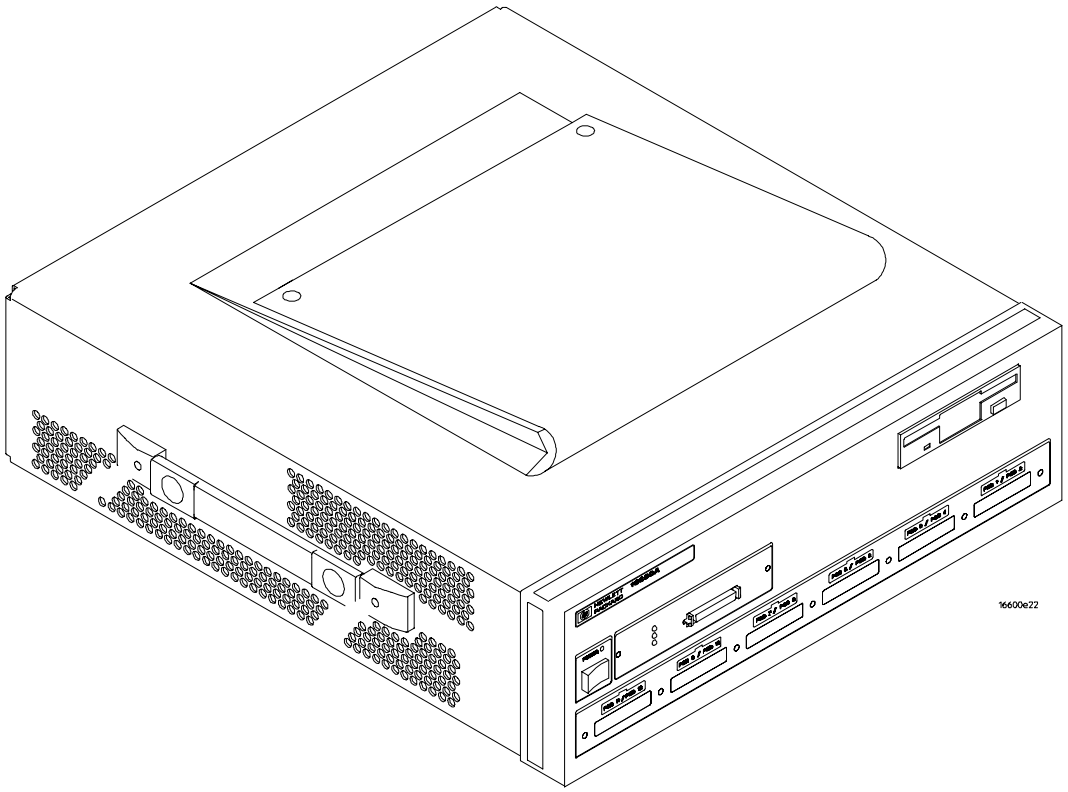
Options

- 160 MByte RAM upgrade
- Color monitor
- CD ROM drive

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the 16600A-series Logic Analysis System.

This instrument can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.



The 16600A-series Logic Analysis System

In This Book

This book is the service guide for the 16600A-series Logic Analysis System and is divided into eight chapters.

Chapter 1 contains information about the instrument and includes accessories for the instrument, specifications and characteristics of the instrument, and a list of the equipment required for servicing the instrument.

Chapter 2 tells how to prepare the instrument for use.

Chapter 3 gives instructions on how to test the performance of the instrument.

Chapter 4 contains calibration instructions for the instrument.

Chapter 5 contains self-tests and flowcharts for troubleshooting the instrument.

Chapter 6 tells how to replace the instrument and assemblies of the instrument, and how to return them to Agilent Technologies.

Chapter 7 lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8 explains how the instrument works and what the self-tests are checking.

Contents

6 Replacing Assemblies

7 Replaceable Parts

8 Theory of Operation

1

General Information

General Information

This chapter lists the accessories, the specifications and characteristics, and the recommended test equipment.

Accessories

The following accessories are supplied with the 16600A-series Logic Analysis System.

Accessories Supplied	Qty
Installation Guide	1
Installation Placemat	1
Mouse	1
Keyboard	1
Power cord	1
CD ROM containing backup composite software	1
Filler Panels	0 or 1, depending on whether a module is ordered with the 16600A-series
Probe Tip Assembly	2

Accessories Available

Other accessories available for the 16600A-series Logic Analysis System are listed in the *Accessories for Logic Analyzers* brochure.

Specifications

The specifications are the performance standards against which the product is tested.

Minimum State Clock Pulse Width: [1]	3.50 ns
Threshold Accuracy:	± (100 mV + 3% of threshold setting)
Minimum Master-to-Master Clock Time: [1]	10.00 ns
Setup/Hold Time:	
Single Clock, Single Edge: [1]	0.0/4.5 ns through 4.5/0.0 ns, adjustable in 500-ps increments
Single Clock, Multiple Edges: [1]	0.0/5.0 ns through 5.0/0.0 ns, adjustable in 500-ps increments
Multiple Clocks, Multiple Edges: [1]	0.0/5.5 ns through 5.5/0.0 ns, adjustable in 500-ps increments

[1] Specified for an input signal VH = –0.9 V, VL = –1.7 V, threshold = –1.3 V, slew rate = 1 V/ns.

Characteristics

These characteristics are not specifications, but are included as additional information. The following characteristics are typical for the 16600A-series system.

Power Requirements

Line Voltage	115 V / 230 V, autoselect
Frequency	48 - 66 Hz
Power	285 W maximum CAT II, Pollution degree 2

Operating Environment

Indoor Use Only

Temperature

Instrument	0 °C to 50 °C (+32 °F to 122 °F).
Disk Media	10 °C to 40 °C (+50 °F to 104 °F).
Probes and Cables	0 °C to 65 °C (+32 °F to 149 °F).

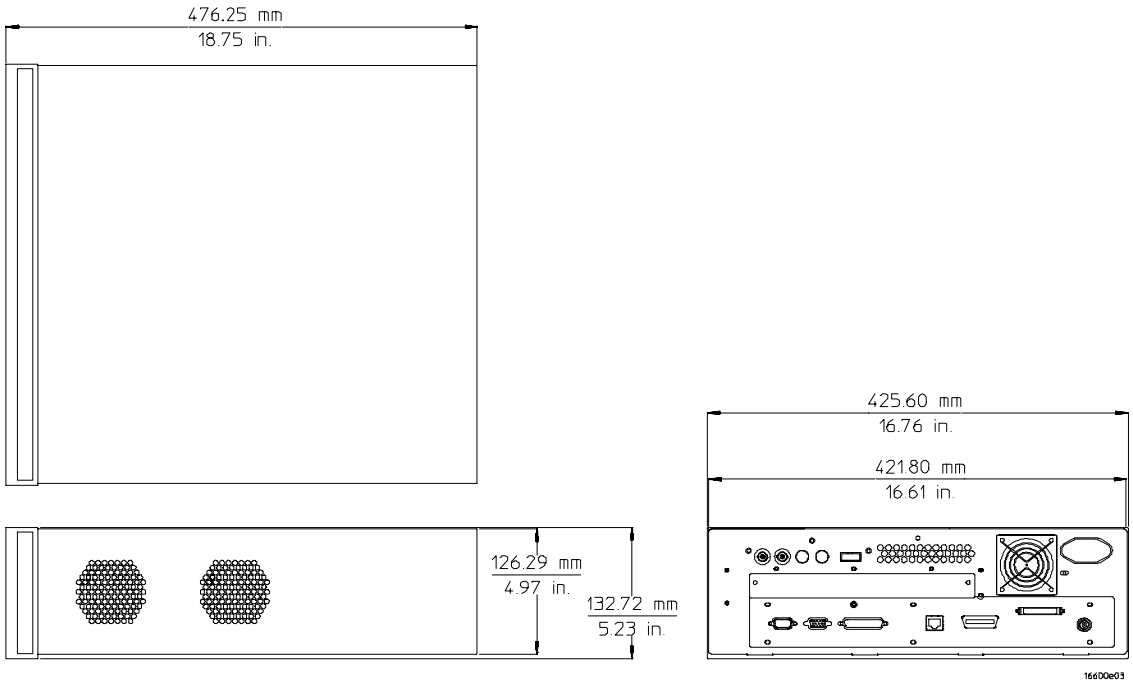
Humidity 8% to 80% relative humidity at 40 °C (104 °F).

Altitude Up to 3000 m (10,000 ft).

Vibration

Operating	Random vibration 5-500Hz, 10 minutes per axis, ~ 0.3 g (rms).
Non-operating	Random vibration 5-500Hz, 10 minutes per axis, ~ 2.41 g (rms); and swept sine resonant search, 5-500Hz, 0.75g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Dimensions Refer to the following figure for dimensional detail.



Dimensional Detail

Recommended test equipment

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part	Use*
Pulse Generator	100 MHz, 3.5 ns pulse width, < 600 ps rise time	8133A Option 003	P,T
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A mainframe with 54751A plugin module	P
Function Generator	Accuracy $\leq(5)(10^{-6}) \times$ frequency, DC offset voltage ±6.3 V	3325B Option 002	P
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A	P
BNC-Banana Cable		11001-60001	P
BNC Tee	BNC (m)(f)(f)	1250-0781	P
Cable	BNC (m-m) 48 inch	8120-1840	P
SMA Coax Cable (Qty 3)	≥ 18 GHz bandwidth	8120-4948	P
Adapter (Qty 4)	SMA(m)-BNC(f)	1250-1200	P
Adapter	SMA(f)-BNC(m)	1250-2015	P
Coupler	BNC (m-m)	1250-0216	P
20:1 Probes (Qty 2)		54006A	P
BNC Test Connector, 17x2 (Qty 1)**			P
BNC Test Connector, 6x2 (Qty 4)**			P,T

*A = Adjustment P = Performance Tests T = Troubleshooting

**Instructions for making these test connectors are in chapter 3, "Testing Performance."

2

Preparing for Use

Preparing For Use

This chapter gives you instructions for preparing the logic analysis system for use.

Power Requirements

The 16600A-series logic analysis system requires a power source of 115 Vac to 230 Vac, –22% to +10%, single phase, 48 to 66 Hz, 285 Watts maximum power. The line voltage is autodetected by the instrument.

Operating Environment

The operating environment is listed in chapter 1. Note the noncondensing humidity limitation below. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analysis system will operate at all specifications within the temperature and humidity range given in chapter 1. However, reliability is enhanced when operating it within the following ranges:

- Temperature: +20 °C to +35 °C (+68 °F to +95 °F)
- Humidity: 20% to 80% noncondensing

Storage

Store or ship the logic analysis system in environments within the following limits:

- Temperature: -40 °C to + 75 °C
- Humidity: Up to 90% at 65 °C
- Altitude: Up to 3,000 meters (10,000 feet)

Protect the system from temperature extremes which cause condensation on the instrument.

To inspect the logic analysis system

1 Inspect the shipping container for damage.

If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

WARNING

Hazardous voltages exist in this instrument. To avoid electrical shock, do not apply power to a damaged instrument.

2 Check the supplied accessories.

Accessories supplied with the logic analysis system are listed in "Accessories" in chapter 1.

3 Inspect the product for physical damage.

Check the logic analysis system and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Agilent Technologies Sales Office. Arrangements for repair or replacement are made, at Agilent Technologies' option, without waiting for a claim settlement.

To apply power

1 Connect the power cord to the instrument and to the power source.

This instrument autodetects the line voltage from 115 VAC to 230 VAC. It is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. Refer to chapter 7, "Replaceable Parts," for option numbers of available power cables.

2 Turn on the power switch located on the front panel.

To configure the monitor

Perform the following steps the first time you set up the instrument. After you complete these steps the monitor should display properly.

1 Connect the monitor, keyboard, and mouse to their rear panel ports.

2 Connect the power cord to the instrument. Apply power to the instrument.

3 Initiate the Monitor Selection mode.

a When the LED on the NUMLOCK key on the keyboard illuminates and remains lit for approximately two seconds, press the [TAB] key (this occurs very soon after power is applied).

b When the Monitor Selection mode is enabled, press the [TAB] key. The CPU will then cycle through the monitor settings.

If none of the monitor selections result in a readable display, it is likely that the monitor is not supported by the instrument.

c When the monitor is readable and the resolution shown matches the resolution of the monitor, press the [ENTER] key, then answer "Y" at the query to confirm the monitor selection.

The instrument will continue the boot process, and a logic analysis session will autolaunch.

To install a measurement module

The following steps give general instructions for installing measurement modules into the 16600A-series Logic Analysis System.

CAUTION

Electrostatic discharge can damage electronic components. Use grounded wrist straps and mats when performing any service to modules.

1. Exit all logic analysis sessions.

   In the Session Manager, select **Shutdown**. In the Powerdown window that appears, select **Powerdown**.
2. When "OK to power down" message appears, turn off the power switch, then unplug the power cord. Disconnect any input or output connections.
3. Remove the card or filler panel that is in the slot intended for the module installation.

   Some modules for the logic analysis system require calibration after installation. Refer to the manuals of individual modules for calibration information.
4. Install the module. Seat the card and tighten the screws.

   Keep applying pressure to the center of the card endplate while tightening the thumbscrews finger-tight.

CAUTION

For correct air circulation, filler panels must be installed in an unused card slot. Correct air circulation keeps the instrument from overheating. Keep any extra filler panels for future use.

5. Plug in the system, then turn it on.

   When you turn on the power switch, the logic analysis system performs power-up tests. After the power-up tests are complete, the screen will show your system configuration.

See Also

Service Guides for the individual modules.

To install an emulation module

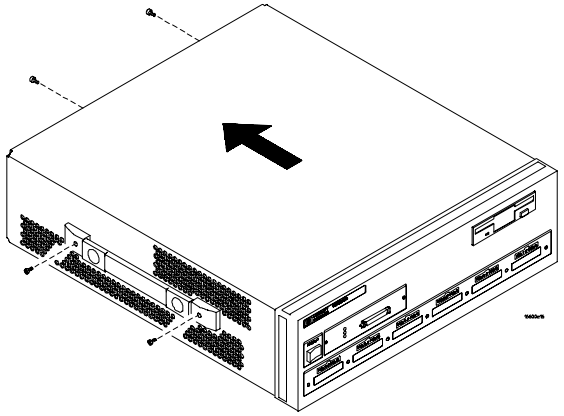
The following steps give general instructions for installing emulation modules into the 16600A-series Logic Analysis System. You will need T-10 and T-15 Torx screwdrivers (supplied with the emulation module). Refer to chapter 6 for additional details on assembly/disassembly procedures.

1 Exit all logic analysis sessions.

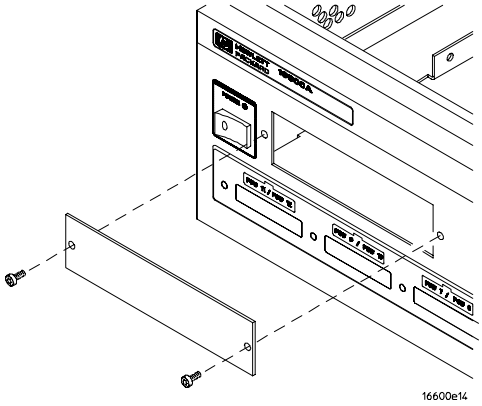
In the Session Manager, select **Shutdown**. In the Powerdown window that appears, select **Powerdown**.

2 When "OK to power down" message appears, turn off the power switch, then unplug the power cord. Disconnect any input or output connections.

3 Slide the cover back.

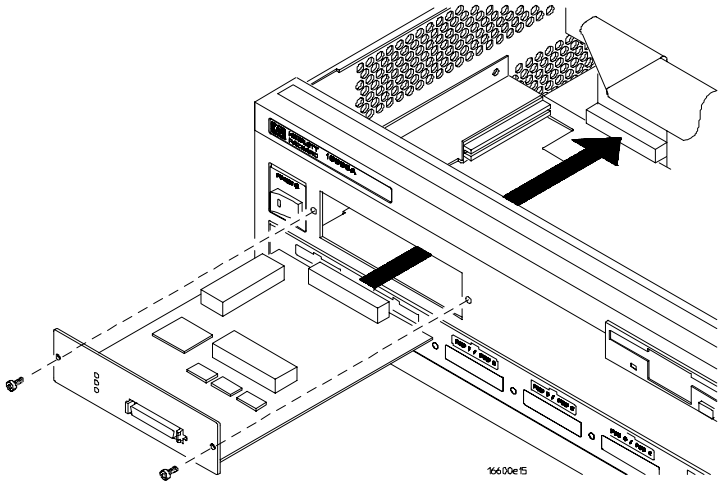


4 Remove the slot cover.



5 Install the emulation module.

6 Connect the cable and re-install the screws.



7 Reinstall the cover.

Tighten the screws snugly (2 N•m or 18 inch-pounds).

8 Plug in the power cord, reconnect the other cables, and turn on the logic analysis system.

The new emulation module will be shown in the system window.

See Also

The "Solutions" manual supplied with your emulation module for information on giving the emulation module a "personality" for your target processor.

Refer to chapter 6 for additional details on assembly/disassembly procedures.

To clean the logic analysis system

- With the instrument turned off and unplugged, use mild soap and water to clean the front and cabinet of the system. Harsh soap might damage the water-base paint.

To test the logic analysis system

The logic analysis mainframe and expansion frame do not require calibration or adjustment.

- If you require a test to initially accept the operation, perform the self-tests in chapter 3, "Testing Performance."
- If the logic analysis system does not operate correctly, go to the beginning of chapter 5, "Troubleshooting."

3

Testing Performance

Testing Performance

This chapter tells you how to test the performance of the logic analyzer against the specifications listed in chapter 1. To ensure the logic analyzer is operating as specified, software tests (self-tests) and manual performance tests are done. The logic analyzer is considered performance-verified if all of the software tests and manual performance tests have passed. The procedures in this chapter indicate what constitutes a "Pass" status for each of the tests.

Self-Tests

The self-tests listed in this chapter check the functional operation of the logic analysis system. Self-tests for the optional modules installed in the frames are listed in the individual module Service Guides.

There are two types of self-tests: self-tests that automatically run at power-up, and self-tests that you select on the screen. For descriptions of the tests, refer to chapter 8, "Theory of Operation."

Perform the self-tests as an acceptance test when receiving the logic analysis system or when the logic analysis system is repaired.

If a test fails, refer to chapter 5, "Troubleshooting."

Test Strategy

For a complete test, start at the beginning with the software tests and continue through to the end of the chapter. For an individual test, follow the procedure in the test.

Test Interval

Test the performance of the module against specifications at two-year intervals.

Test Record Description

A performance test record for recording the results of each procedure is located at the end of this chapter. Use the performance test record to gauge the performance of the module over time.

Test Equipment

Each procedure lists the recommended test equipment. You can use equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number.

Instrument Warm-Up

Before testing the performance of the module, warm-up the instrument and the test equipment for 30 minutes.

Perform the Self-tests

There are two types of self-tests: self-tests that automatically run at power-up, and self-tests that you select on the screen. The self-tests verify the correct operation of the logic analysis system. Self-tests can be performed all at once or one at a time. While testing the performance of the logic analysis system, run the self-tests all at once.

To perform the power-up tests

The logic analysis system automatically performs power-up tests when you apply power to the instrument. Any errors are reported in the boot dialogue. Serious errors will interrupt the boot process.

The power-up tests are designed to complement the instrument on-line Self Tests. Tests that are performed during power-up are not repeated in the Self Tests.

The monitor, keyboard and mouse must be connected to the mainframe to observe the results of the power-up tests.

1. Disconnect all inputs and exit all logic analysis sessions.

   In the Session Manager, select **Shutdown**. In the Powerdown window, select **Powerdown**.
2. When the "OK to power down" message appears, turn off the power switch.
3. After a few seconds, turn the power switch back on. Observe the boot dialogue for the following:
   - ensure all of the installed memory is recognized
   - any error messages
   - interrupt of the boot process with or without error message

   A complete transcript of the boot dialogue is in Chapter 8, "Theory of Operation".
4. During initialization, check for any failures.

   If an error or an interrupt occurs, refer to Chapter 5, "Troubleshooting".

To perform the self-tests

The self-tests verify the correct operation of the logic analysis system. Self-tests can be performed all at once or one at a time. While testing the performance of the logic analysis system, run the self-tests all at once.

1 Launch the Self-Tests.
   - **a** In the System window, click on System Admin.
   - **b** In the System Administration window, click on Self-Test . . .
   - **c** In the query pop-up, select Yes to exit the current session.

     The Self-Test closes down the current session because the test algorithms leave the system in an unknown state. Re-launching a session at the end of the tests will ensure the system is properly initialized.

2 In the Self-Test window select Test All.

   When the tests are finished, the Status will change to TEST passed or TEST failed. You can find detailed information about the test results in the Status Message field of the Self-Test window.

   The System CPU Board test returns Untested because the CPU tests require user action. To test the CPU Board, select CPU Board, then select each test individually.

   For more information on the tests that are not executed, refer to Chapter 8.

3 Select Quit to exit the Test menu.

4 In the Session Manager, select Start Session This Display to re-launch a logic analysis session.

Make the Test Connectors

The test connectors connect the logic analysis system to the test equipment.

Materials Required

Description	Recommended Agilent Part	Qty
BNC (f) Connector	1250-1032	4
100 Ω 1% resistor	0698-7212	6
Berg Strip, 17-by-2		1
Berg Strip, 6-by-2		3
20:1 Probe	54006A	2
Jumper wire		

1 Build three test connectors using BNC connectors and 6-by-2 sections of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

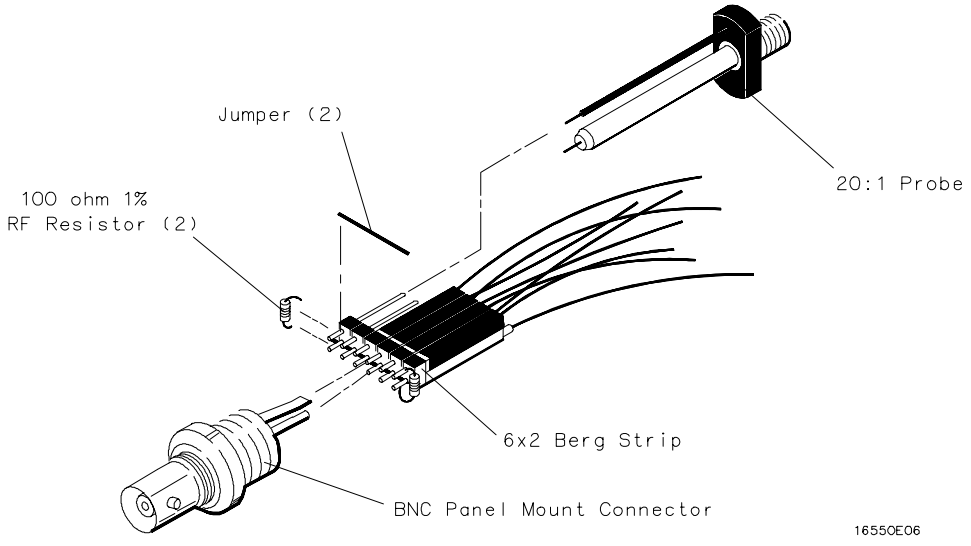
b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder two resistors to the Berg strip, one at each end between the end pins.

d Solder the center of the BNC connector to the center pin of one row on the Berg strip.

e Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.

f On two of the test connectors, solder a 20:1 probe. The probe ground goes to the same row of pins on the test connector as the BNC ground tab.



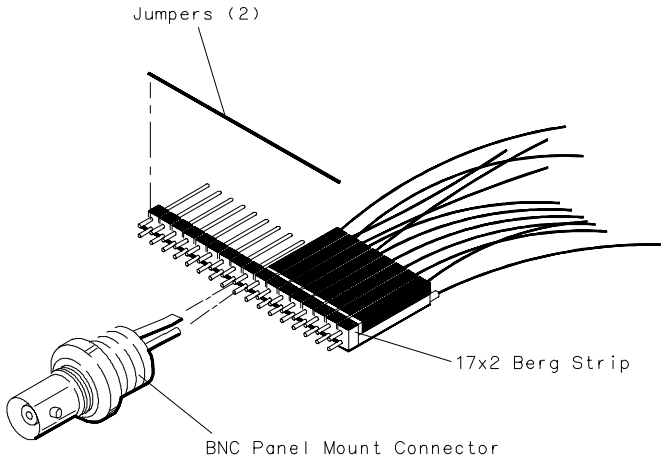
2 Build one test connector using a BNC connector and a 17-by-2 section of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder the center of the BNC connector to the center pin of one row on the Berg strip.

d Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.



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To Set up the Test Equipment and the Analyzer

Before testing the specifications of the 16600A-series logic analysis system, the test equipment and the logic analysis system must be set up and configured.

These instructions include detailed steps for initially setting up the required test equipment and the logic analysis system. Before performing any or all of the following tests in this chapter, the following steps must be followed.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, <600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, <58 ps rise time	54750A w/ 54751A
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A
Function Generator	DC offset voltage ±6.3 V	3325B Option 002

Set up the equipment

1. Turn on the required test equipment listed in the table above. Let them warm up for 30 minutes before beginning any test.
2. Turn on the logic analysis system.
   - **a** Connect the keyboard, mouse, and monitor to the rear panel of the logic analysis system mainframe.
   - **b** Plug in the power cord to the power connector on the rear panel of the mainframe.
   - **c** Turn on the main power switch on the mainframe front panel.
3. Set up the logic analysis system.
   - **a** Open the Session Manager window and select "Start Session on This Display".
   - **b** In the Logic Analysis System window, select Navigate, then select Slot A: MACHINE 1, then select Setup. A Setup window will now open.
   - **c** In the MACHINE 1 Setup window, select Navigate, then select Slot A: MACHINE 1, then select Listing. A Listing window will open.
   - **d** In the MACHINE 1 Setup window, select the Config tab.
4. Set up the pulse generator according to the following table.

Timebase	Channel 2	Trigger	Channel 1
Mode: Int Period: 10.000 ns	Mode: Pulse Divide: PULSE ÷ 2 Width: 4.500 ns High: -0.90 V Low: -1.70 V COMP: Disabled (LED Off)	Divide: Divide ÷ 2 Ampl: 0.50 V Offs: 0.00 V	Mode: Pulse Delay: 0.000 ns Width: 3.500 ns High: -0.90 V Low: -1.70 V COMP: Disabled (LED Off)

5 Set up the oscilloscope.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	**Display**	**Trigger**	**[Shift] Δ Time**
Averaging: On # of averages: 16	Graticule Graphs: 2	Level: 0.0 mV	Stop src: channel 2 [Enter]

Channel 1	**Channel 2**	**Define meas**
External Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: –1.300 V	External Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: -1.300 V	Thresholds: user-defined Units: Volts Upper: -980 mV Middle: -1.30 V Lower: -1.62 V

Allow the logic analysis system to warm up for 30 minutes before beginning any of the following tests.

To Test the Threshold Accuracy

Testing the threshold accuracy verifies the performance of the following specification:

- Clock and data channel threshold accuracy

These instructions include detailed steps for testing the threshold settings of Pod A1. After testing Pod A1, connect and test the rest of the pods one at a time. To test the next pod, follow the detailed steps for Pod A1, substituting the next pod for Pod A1 in the instructions.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A
Function Generator	DC offset voltage ±6.3 V	3325B Option 002
BNC-Banana Cable		11001-60001
BNC Tee		1250-0781
BNC Cable		8120-1840
BNC Test Connector, 17x2		

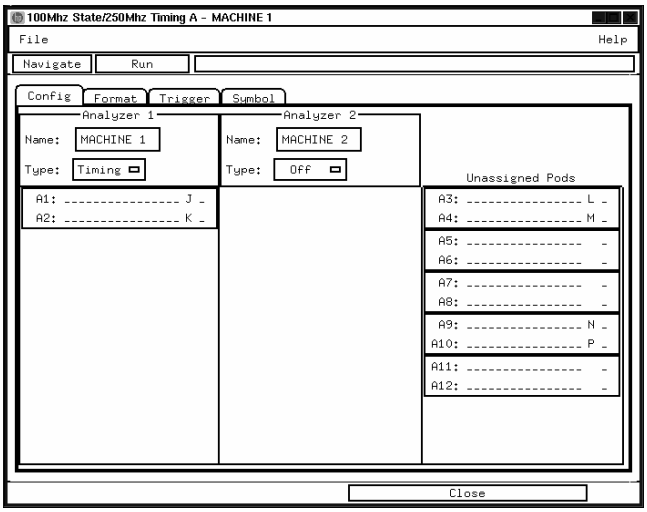
Set up the equipment

1. If you have not already done so, perform the procedure described in "To Set up the Test Equipment and the Analyzer".
2. Set up the function generator.
   a. Set up the function generator to provide a DC offset voltage at the Main Signal output.
   b. Disable any AC voltage to the function generator output, and enable the high voltage output.
   c. Monitor the function generator DC output voltage with the multimeter.

Set up the logic analyzer

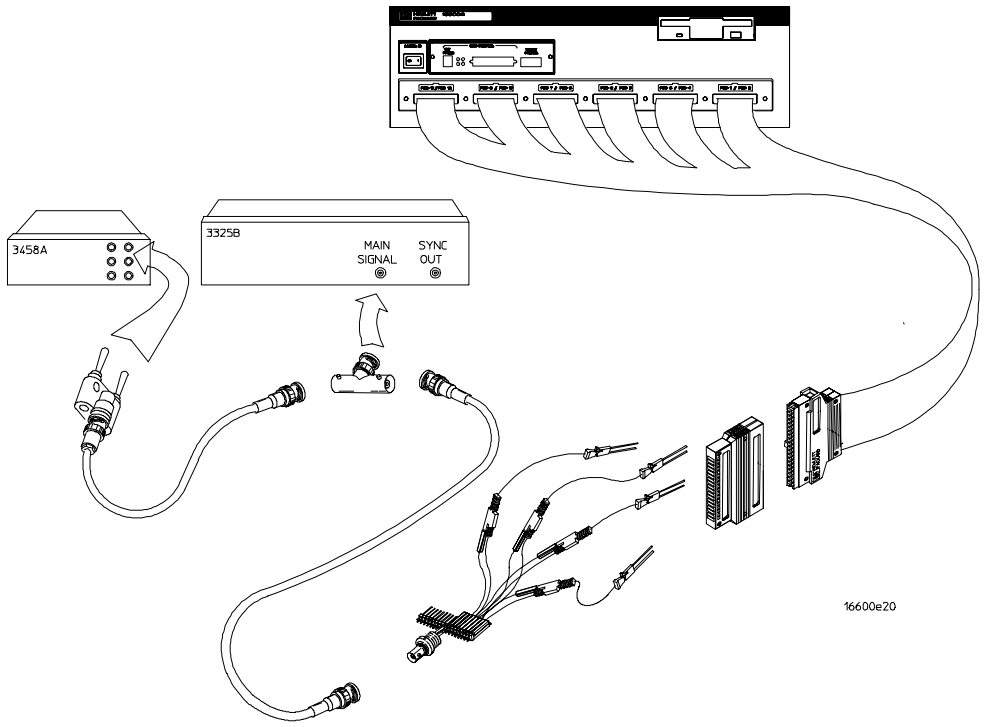
1 In the MACHINE 1 Setup window, select the Config tab.

2 Under the Config tab, unassign the pods that are assigned to Analyzer 2. To unassign the pods, use the mouse to drag the pods to the Unassigned Pods column.



Connect the logic analyzer

1. Using the 17-by-2 test connector, BNC cable, and probe tip assembly, connect the data and clock channels of Pod A1 to one side of the BNC Tee.
2. Using a BNC-banana cable, connect the voltmeter to the other side of the BNC Tee.
3. Connect the BNC Tee to the Main Signal output of the function generator.

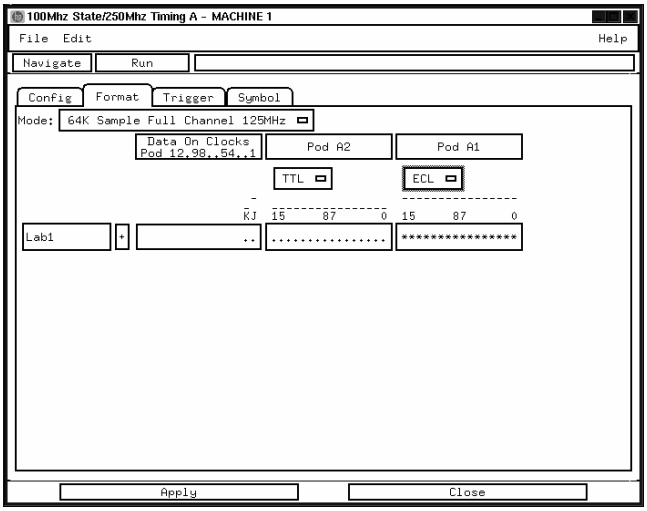


Test the ECL threshold

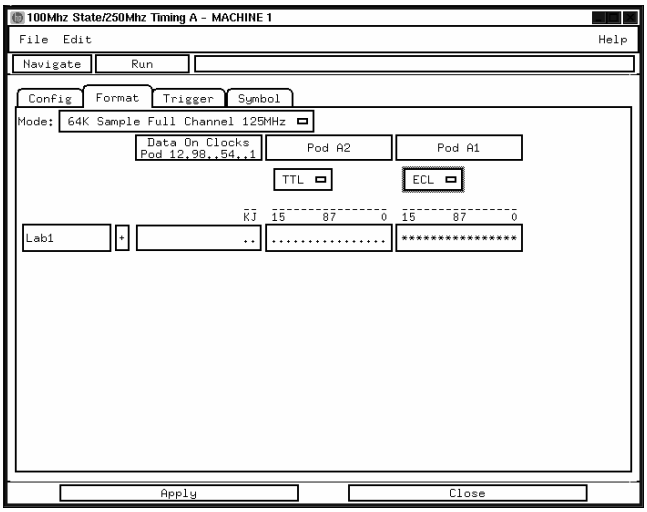
1 Under the Format tab, select the threshold field for the pod under test, then select ECL.

2 On the function generator front panel, enter –1.159 V ±1 mV DC offset. Use the multimeter to verify the voltage.

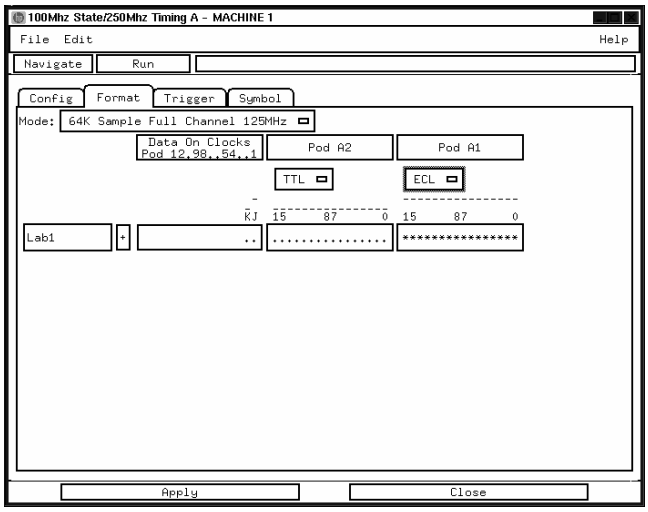
The activity indicators for Pod A1 should show all data channels and the J-clock channel at a logic high.



3 Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for the pod under test show the channels are at a logic low. Record the function generator voltage in the performance test record.



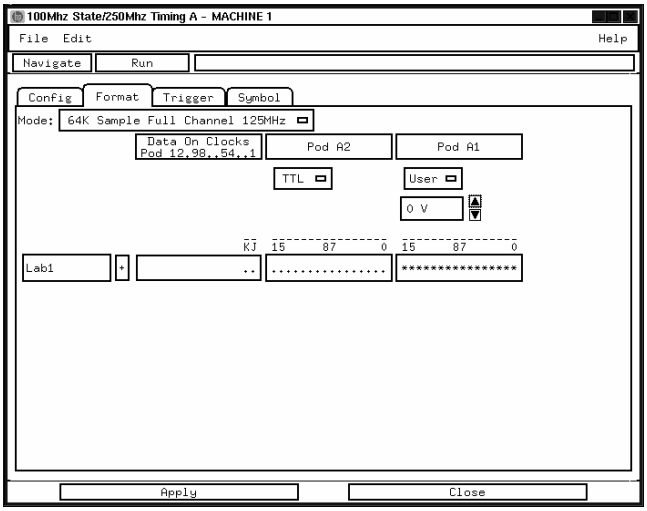
4 Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for the pod under test show the channels are at a logic high. Record the function generator voltage in the performance test record.



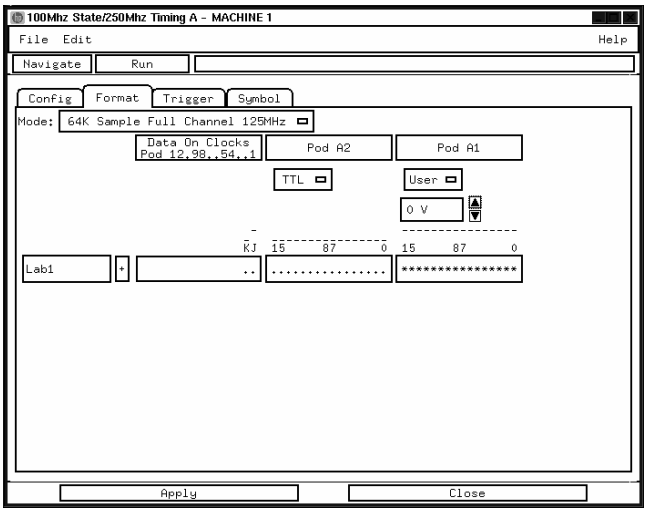
Test the 0 V User threshold

1. Under the Format tab, select the threshold field, then select User. In the numeric field, enter 0 V.
2. On the function generator front panel, enter +0.102 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for the pod under test should show all data channels and the J-clock channel at a logic high.
3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for the pod under test show the channels at a logic low. Record the function generator voltage in the performance test record.



4. Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for the pod under test show the channels at a logic high. Record the function generator voltage in the performance test record.



Test the next pod

Using the 17-by-2 test connector and probe tip assembly, connect the data and clock channels of the next pod to the output of the function generator as shown in "Connect the logic analyzer". If you have just finished testing Pod A1, connect the data and clock channels of Pod A2. Repeat until all pods have been tested.

Note that the pod under test must be assigned to the analyzer. For Pod A3, use the MACHINE 1 Setup menu under the Config tab, unassign Pods A1 and A2 and assign Pods A3 and A4 to Analyzer 1. Repeat this unassignment and assignment each time you test an odd-numbered pod.

When you have finished testing the last pod, you have completed the threshold accuracy test.

To Test the Single-clock, Single-edge, State Acquisition

Testing the single-clock, single-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time
- Minimum clock pulse width

This test checks a combination of data channels using a single-edge clock at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, <600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, <58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)		8120-4948
Coupler (Qty 3)	BNC(m-m)	1250-0216
BNC Test Connector, 6x2 (Qty 3)		

Set up the equipment

If you have not already done so, do the procedure "To Set up the Test Equipment and the Analyzer". Ensure that the pulse generator and oscilloscope are set up according to the tables in that section.

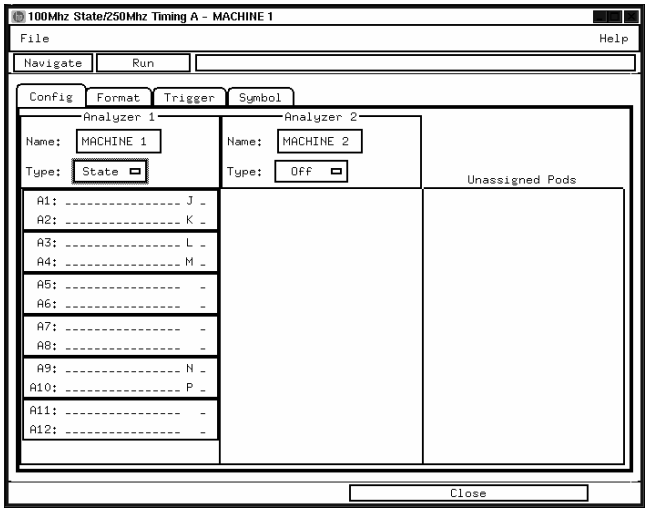
Set up the logic analyzer

1 Set up the Configuration window.

a In the MACHINE 1 window, select the Config tab.

b In the Analyzer 1 Type box select Timing, then in the pop-up menu select State.

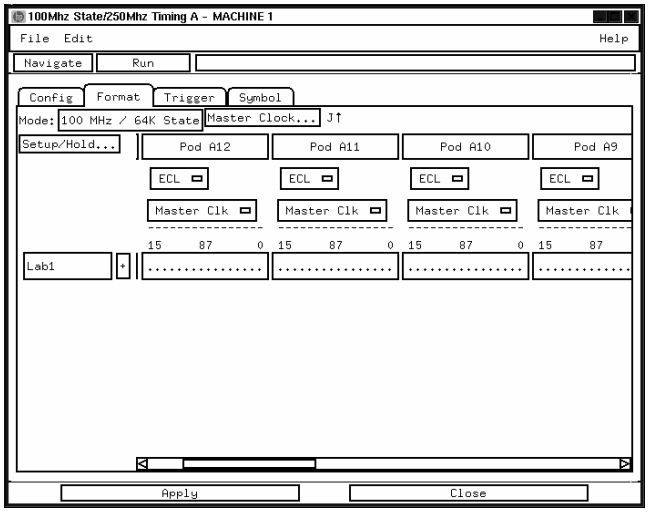
2 Under the Config tab, assign all pods to Analyzer 1. To assign the pods, use the mouse to drag the pods to the Analyzer 1 column.



3 Set up the Format window.

a In the MACHINE 1 setup window, select the Format tab.

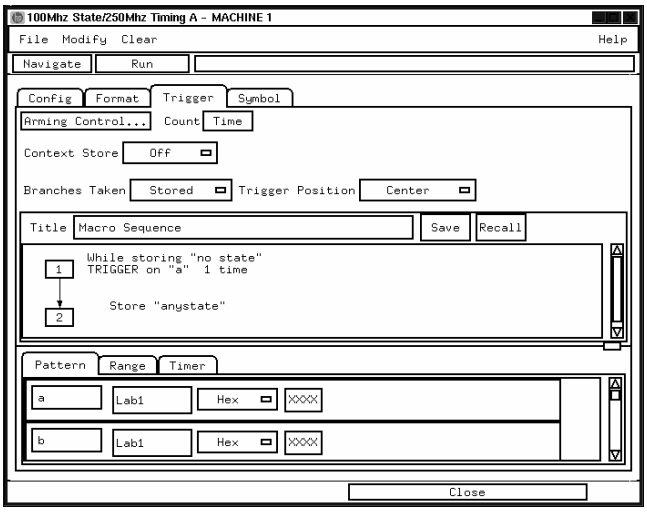
b Under each Pod field, select TTL, then select ECL. The screen does not show all pod fields at one time. To access more pod fields, use the scroll bars of the MACHINE 1 window.



4 Set up the Trigger window.

a In the MACHINE 1 setup window, select the Trigger tab. Under the Trigger tab, select the Pattern tab at the bottom of the window.

b Click and hold the field labeled "1" in the Sequence field, then slide the cursor to Edit and release the mouse. In the pop-up window, select "anystate", then select "no state". Select Close.

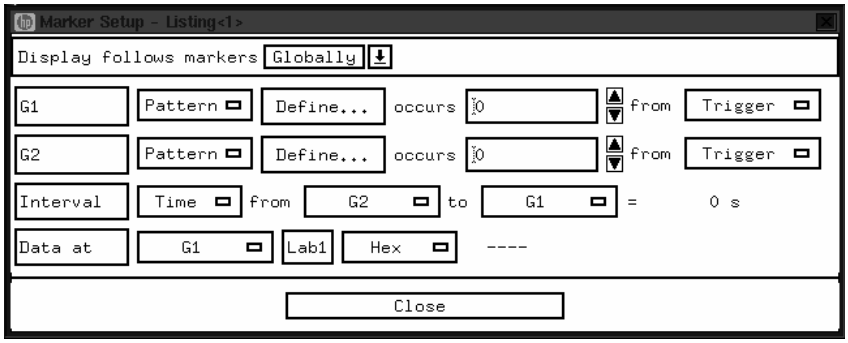


5 Set up the Listing window.

a In the Listing window, select the Markers tab.

b Select the G1: field and the Markers Setup window will appear.

c Select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select Pattern.

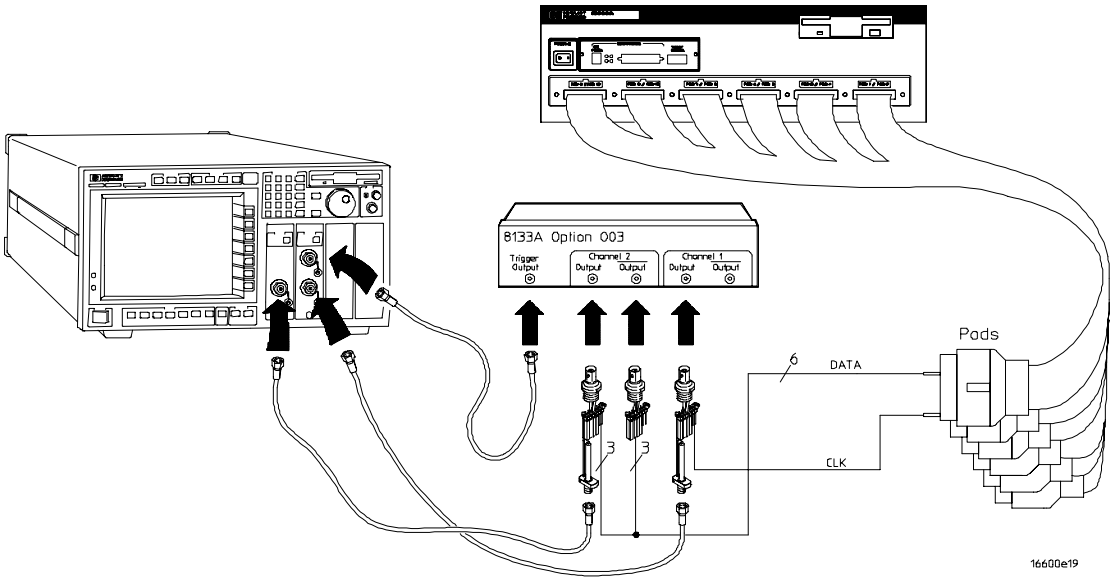


Note: Leave the Marker Setup window open. You will be entering numeric values in the "occurs" field after acquiring the test data.

Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following tables to the pulse generator. Note that this procedure is repeated several times for this test, and each time you use a different set of channels. There is also a different set of tables for each 16600A-series logic analysis system.

2 Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator according to the following illustration. Use the data and clock according to the table for your logic analysis system.



Connect the 16600A to the Pulse Generator

8133A Ch2 OUTPUT	8133A Ch2 $\overline{\text{OUTPUT}}$	8133A Ch1 OUTPUT
First time through this procedure		
Pod A1 channel 3 Pod A5 channel 3 Pod A9 channel 3	Pod A3 channel 3 Pod A7 channel 3 Pod A11 channel 3	J-clock
Second time through this procedure		
Pod A1 channel 11 Pod A5 channel 11 Pod A9 channel 11	Pod A3 channel 11 Pod A7 channel 11 Pod A11 channel 11	J-clock
Third time through this procedure		
Pod A2 channel 3 Pod A6 channel 3 Pod A10 channel 3	Pod A4 channel 3 Pod A8 channel 3 Pod A12 channel 3	J-clock
Fourth time through this procedure		
Pod A2 channel 11 Pod A6 channel 11 Pod A10 channel 11	Pod A4 channel 11 Pod A8 channel 11 Pod A12 channel 11	J-clock

Connect the 16601A to the Pulse Generator

8133A Ch2 OUTPUT	8133A Ch2 $\overline{\text{OUTPUT}}$	8133A Ch1 OUTPUT
First time through this procedure		
Pod A1 channel 3	Pod A2 channel 3	J-clock
Pod A3 channel 3	Pod A4 channel 3	
Pod A5 channel 3	Pod A6 channel 3	
Pod A7 channel 3	Pod A8 channel 3	
Second time through this procedure		
Pod A1 channel 11	Pod A2 channel 11	J-clock
Pod A3 channel 11	Pod A4 channel 11	
Pod A5 channel 11	Pod A6 channel 11	
Pod A7 channel 11	Pod A8 channel 11	

Connect the 16602A to the Pulse Generator

8133A Ch2 OUTPUT	8133A Ch2 $\overline{\text{OUTPUT}}$	8133A Ch1 OUTPUT
First time through this procedure		
Pod A1 channel 3	Pod A2 channel 3	J-clock
Pod A3 channel 3	Pod A4 channel 3	
Pod A5 channel 3	Pod A6 channel 3	
Second time through this procedure		
Pod A1 channel 11	Pod A2 channel 11	J-clock
Pod A3 channel 11	Pod A4 channel 11	
Pod A5 channel 11	Pod A6 channel 11	

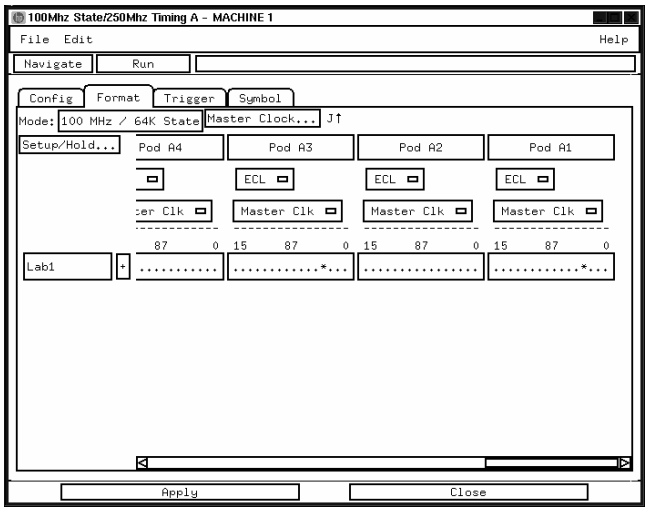
Connect the 16603A to the Pulse Generator

8133A Ch2 OUTPUT	8133A Ch2 $\overline{\text{OUTPUT}}$	8133A Ch1 OUTPUT
Pod A1 channel 3	Pod A1 channel 11	J-clock
Pod A2 channel 3	Pod A2 channel 11	
Pod A3 channel 3	Pod A3 channel 11	
Pod A4 channel 3	Pod A4 channel 11	

3 Activate the data channels that are connected according to the previous table.

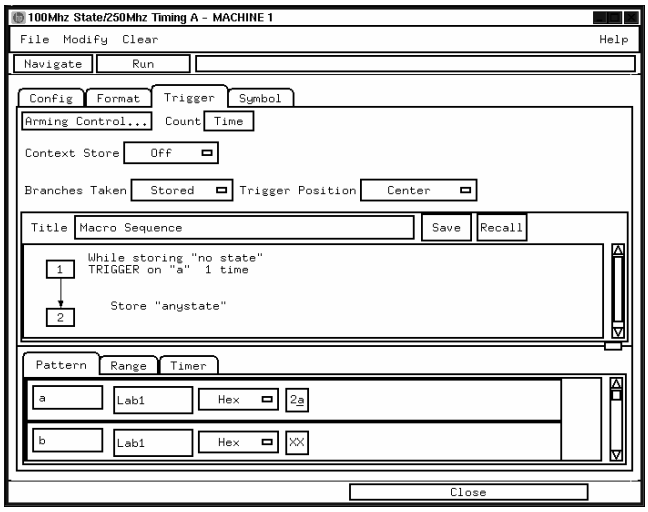
a In the MACHINE 1 setup window, select the Format tab.

b Under the Format tab, select the field showing the channel assignments for one of the pods being tested. Using the mouse, select the data channel to be tested. An asterisk means that a channel is turned on. Follow this step for the remaining pods to be tested.



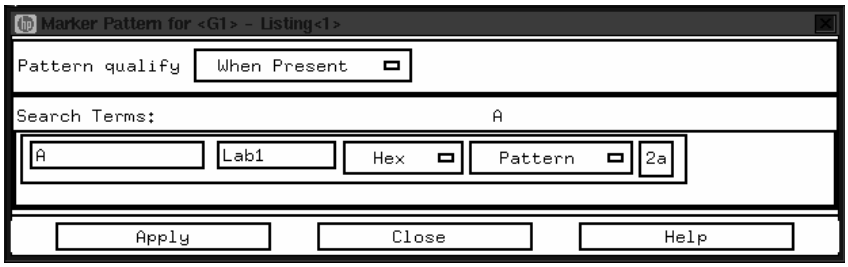
c Under the Trigger tab, select the pattern field associated with pattern recognizer "a". Delete the "XX" and enter the pattern shown below for your analyzer.

Logic Analysis System	Pattern
16600A, 16602A	"2a"
16601A, 16603A	"aa"



d In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window will appear. In the pattern field, enter the value according to the following table. Select Apply, then select Close.

Analyzer	Pattern
16600A, 16602A	"2a"
16601A, 16603A	"aa"



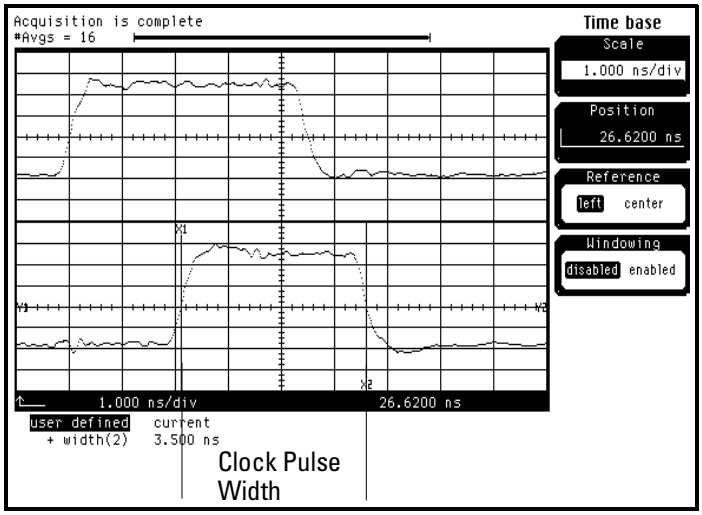
e In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window will appear. In the pattern field, enter the value according to the following table. Select Apply, then select Close.

Analyzer	Pattern
16600A, 16602A	"15"
16601A, 16603A	"55"

Verify the test signal

1 Check the clock pulse width. Using the oscilloscope, verify that the clock pulse width is 3.500 ns, +0 ps or -100 ps.

- **a** Enable the pulse generator channel 1, channel 2, and trigger outputs (LED off).
- **b** In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.
- **c** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that the waveform is centered on the screen.
- **d** On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the clock signal pulse width (+ width(2)).
- **e** If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



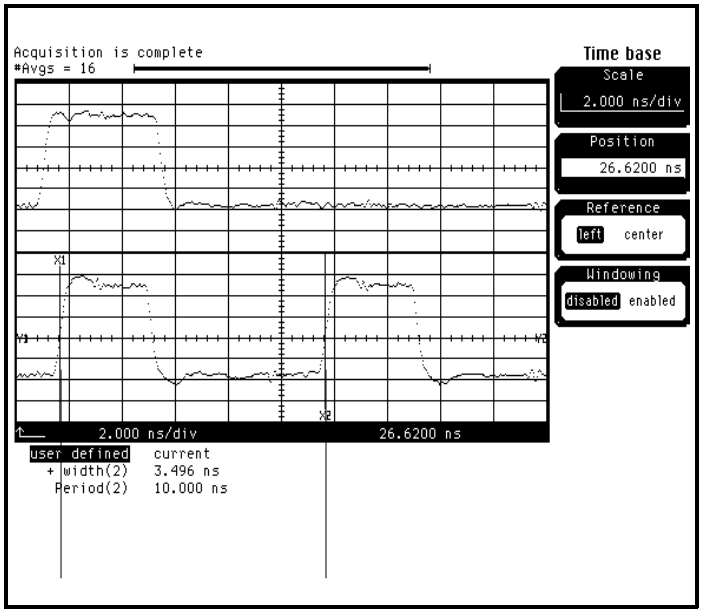
2 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns.

a In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

c On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is not less than 10.000 ns, go to step d. If the period is less than 10.000 ns, go to step 3.

d In the oscilloscope Timebase menu, increase Position 10.000 ns. If the period is not less than 10.000 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than 10.000 ns.



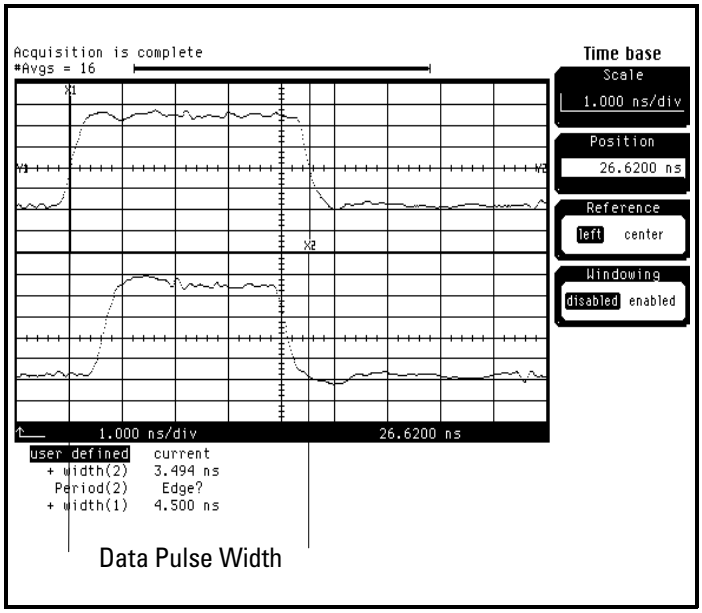
3 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 4.500 ns, +0 ps or -100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold combination

1 Select the logic analyzer setup/hold time.

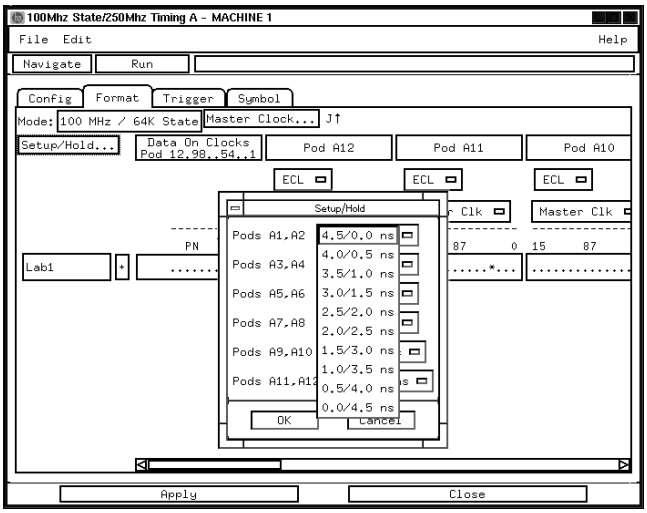
a In the MACHINE 1 setup window, select the Format tab.

b Under the Format tab, select Setup/Hold.

c In the Setup/Hold window, select the setup/hold field next to each pod pair, then select the setup/hold combination to be tested. Repeat for all pods.

The first time through this test, select the top combination in the following table.

Setup/Hold Combinations
4.5/0.0 ns
0.0/4.5 ns



d Select OK to exit the Setup/Hold window.

2 Disable the pulse generator channel 1 COMP (LED off).

3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: rising.

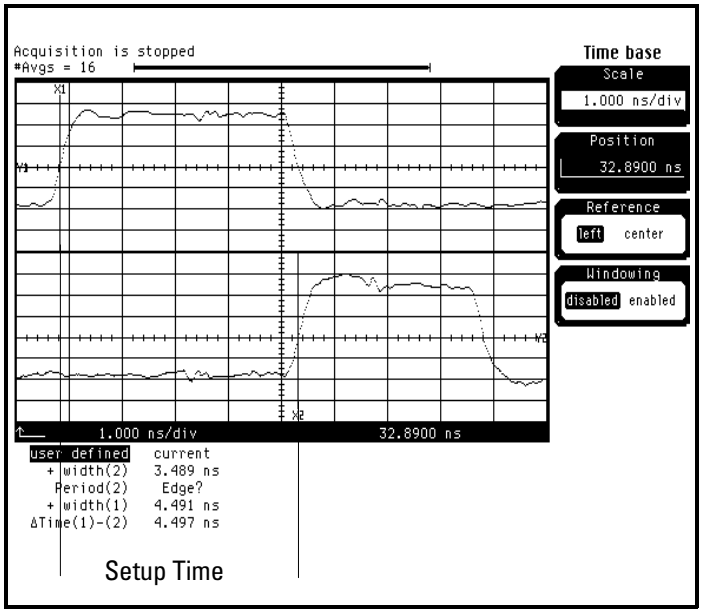
b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position both a clock and a data waveform on the display, with the rising edge of the clock waveform centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (ΔTime(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.

Data Signal

Clock Signal



4 Select the clock to be tested.

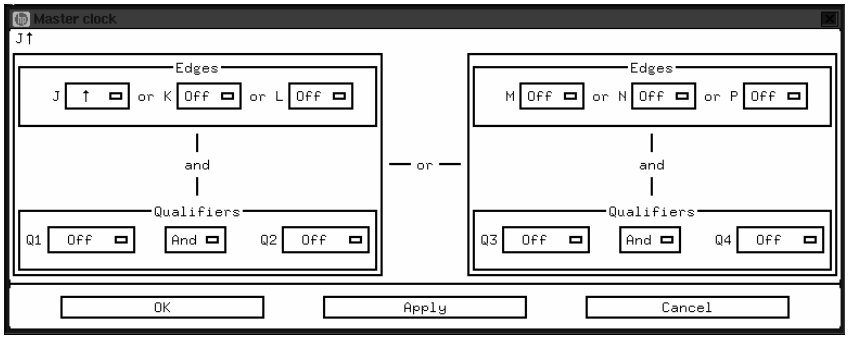
a In the MACHINE 1 setup window under the Format tab, select Master Clock . . .

b In the Master Clock window, select the edge field next to the clock to be tested, then select the clock edge as indicated in the table. Turn off all other clocks.

The first time through this test, select the first clock and edge.

Clocks

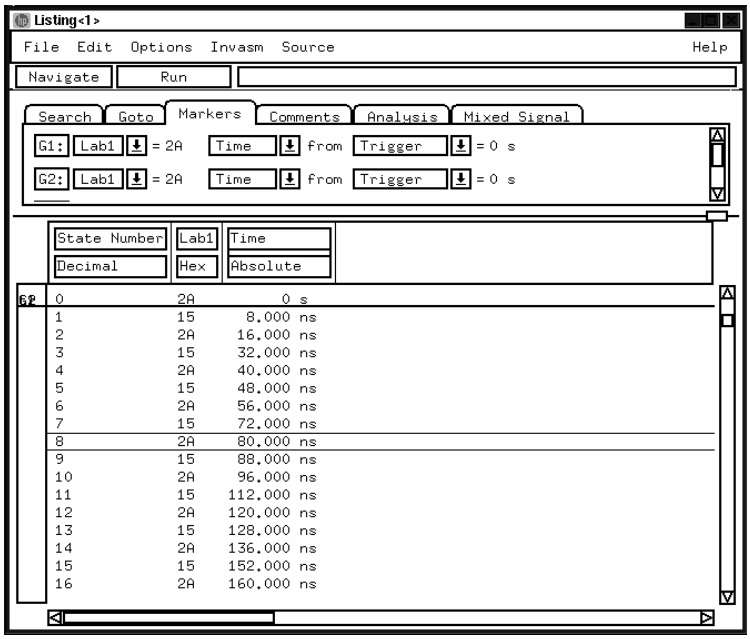
Analyzer	Clocks					
16600A, 16601A, 16602A	J↑	K↑	L↑	M↑	N↑	P↑
16603A	J↑	K↑	L↑	M↑		



c Select Apply.

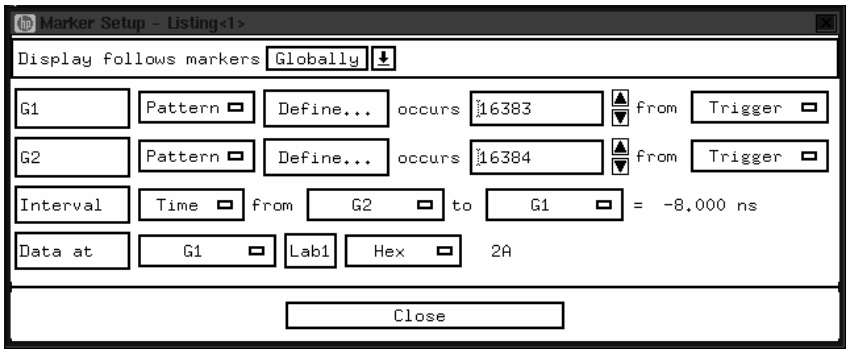
5 Verify the test data.

a In the Listing window, select Run. The display should show an alternating pattern of "2A" and "15" (16600A, 16602A) or "AA" and "55" (16601A, 16603A).



b In the Marker Setup window, select the 'occurs' value field that corresponds to marker G1. Enter 16383.

c In the Marker Setup window, select the 'occurs' value field that corresponds to marker G2. Enter 16384.



d Select Close to apply the marker values to the data. If the "Pattern NOT found for marker..." error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

6 Test the next clock.

a In the MACHINE 1 setup window under the Format tab, select Master Clock . . .

b Repeat steps 4, 5, and 6 for the next clock edge listed in the table in step 4, until all listed clock edges have been tested.

7 Enable the pulse generator channel 1 COMP (LED on).

8 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: falling.

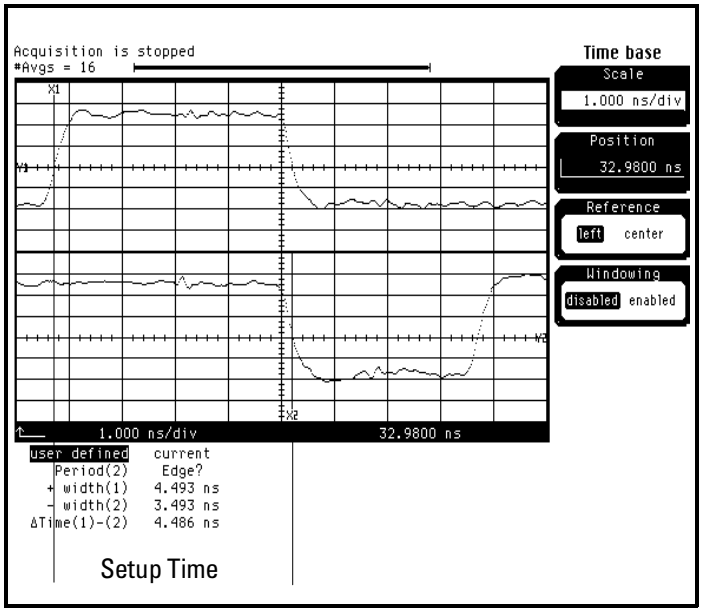
b On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] to verify the clock signal pulse width (- width(2)). If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the clock pulse width is 3.500 ns, +0 ps or -100 ps.

c On the oscilloscope, select [Shift] ΔTime. Select Start src: channel 1, then select [Enter] to display the setup time (ΔTime(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.

Data Signal

Clock Signal



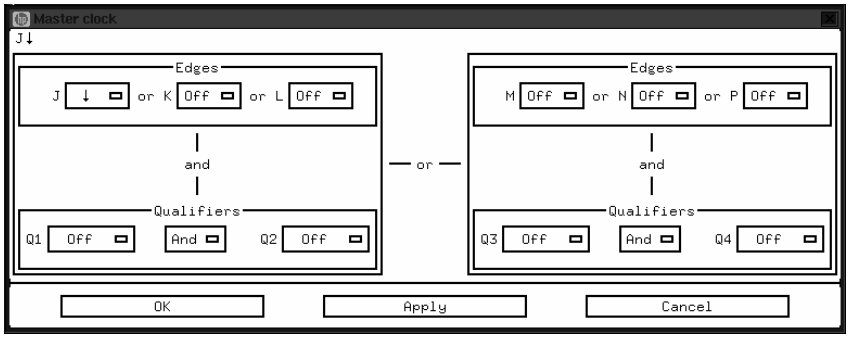
9 Select the clock to be tested.

a In the MACHINE 1 setup window under the Format tab, select Master Clock . . .

b In the Master Clock window, select the edge field next to the clock to be tested, then select the clock edge as indicated in the table. The first time through this test, select the first clock and edge. Ensure all other clocks are turned off.

Clocks

Analyzer	Clocks					
16600A, 16601A, 16602A	J↓	K↓	L↓	M↓	N↓	P↓
16603A	J↓	K↓	L↓	M↓		



c Connect the clock input channel to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

d Select Apply, then select OK to exit the Master Clock menu.

10 Verify the test data.

a In the Listing window, select Run. The display should show an alternating pattern of "2A" and "15" (16600A, 16602A) or "AA" and "55" (16601A, 16603A).

b If the "Pattern NOT found for marker..." error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

11 Test the next clock.

a In the MACHINE 1 setup window under the Format tab, select Master Clock . . .

b Repeat steps 9, 10, and 11 for the next clock edge listed in the table in step 9, until all listed clock edges have been tested.

12 If the setup/hold used for the previous steps was 4.5/0.0 ns, repeat steps 1 through 12 using setup/hold 0.0/4.5 ns. If the setup/hold used for the previous steps was 0.0/4.5 ns, continue on with the next section.

Test the next channels (16600A, 16601A, 16602A)

Connect the next combination of data channels and clock channels, and test them.

Starting with "Connect the logic analyzer," connect the next combination, then continue through the complete test. Repeat until all data channel combinations have been tested.

To Test the Multiple-clock, Multiple-edge, State Acquisition

Testing the multiple-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time
- Minimum clock pulse width

This test checks a combination of data channels using multiple clocks at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, <600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, <58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)		8120-4948
Coupler (Qty 3)	BNC(m-m)	1250-0216
BNC Test Connector, 6x2 (Qty 3)		

Set up the equipment

1 If you have not already done so, do the procedure "To Set up the Test Equipment and the Analyzer". Ensure that the pulse generator and oscilloscope are set up according to the tables in that section.

2 Change the pulse generator channel 1 width to 5.500 ns.

Set up the logic analyzer

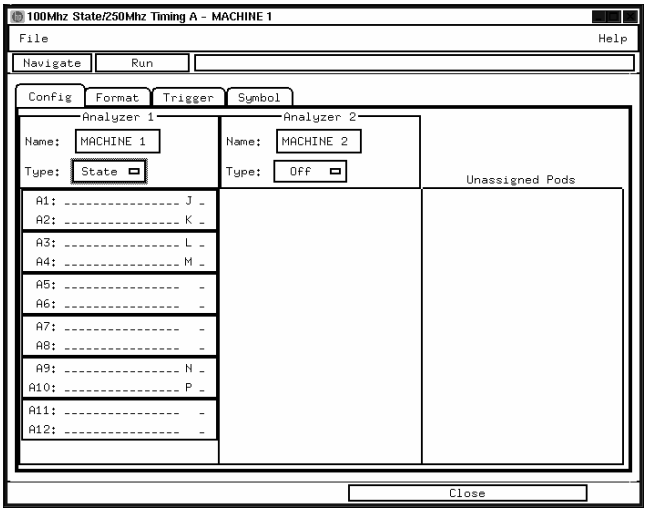
Perform the following steps if you have not already done so for the previous test.

1 Set up the Configuration window.

a In the MACHINE 1 window, select the Config tab.

b In the Analyzer 1 box, select Timing, then in the pop-up menu select State.

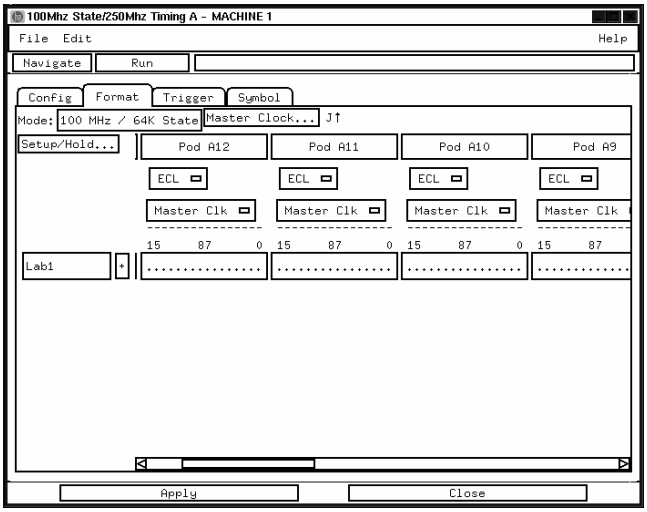
2 Under the Config tab, assign all pods to Analyzer 1. To assign the pods, use the mouse to drag the pods to the Analyzer 1 column.



3 Set up the Format window.

a In the MACHINE 1 setup window, select the Format tab.

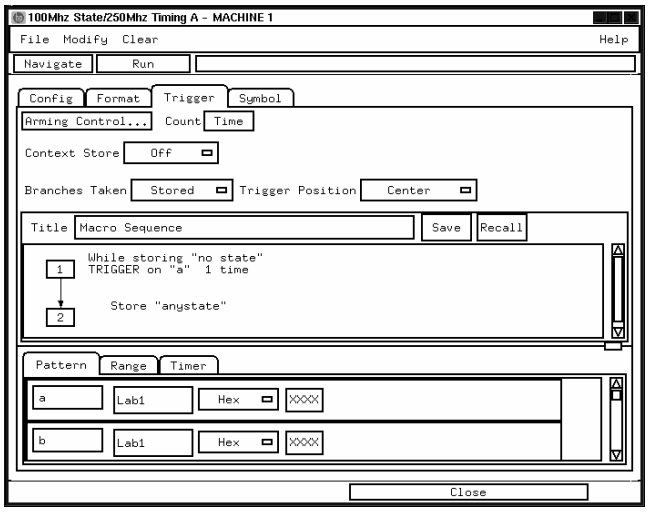
b Under each Pod field, select TTL, then select ECL. The screen does not show all pod fields at one time. To access more pod fields, use the scroll bars of the MACHINE 1 window.



4 Set up the Trigger window.

a In the MACHINE 1 setup window, select the Trigger tab. Under the Trigger tab, select the Pattern tab at the bottom of the window.

b Click and hold the field labeled "1" in the Sequence field, then slide the cursor to Edit and release the mouse. In the pop-up window, select "anystate", then select "no state". Select Close.

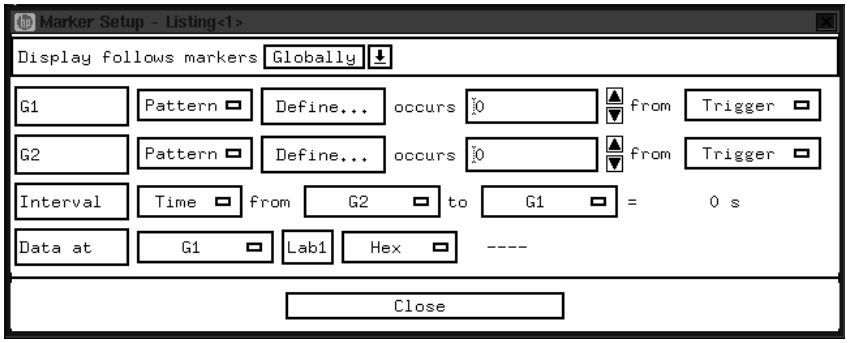


5 Set up the Listing window.

a In the Listing window, select the Markers tab.

b Select the G1: field and the Markers Setup window will appear.

c Select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select Pattern.

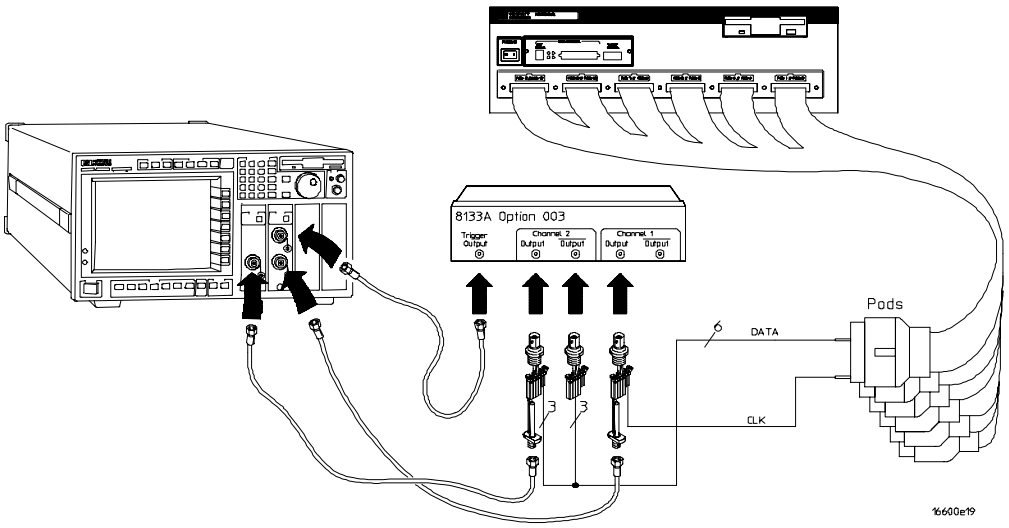


Note: Leave the Marker Setup window open. You will be entering numeric values in the "occurs" field after acquiring the test data.

Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following tables to the pulse generator. Note that this procedure is repeated several times for this test, and each time you use a different set of channels. There is also a different set of tables for each 16600A-series logic analysis system.

2 Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator according to the following illustration. Use the data and clock according to the table for your logic analysis system.



Connect the 16600A to the Pulse Generator

8133A Ch2 OUTPUT	8133A Ch2 $\overline{\text{OUTPUT}}$	8133A Ch1 OUTPUT
First time through this procedure		
Pod A1 channel 3	Pod A3 channel 3	J-clock
Pod A5 channel 3	Pod A7 channel 3	L-clock
Pod A9 channel 3	Pod A11 channel 3	N-clock
Second time through this procedure		
Pod A1 channel 11	Pod A3 channel 11	J-clock
Pod A5 channel 11	Pod A7 channel 11	L-clock
Pod A9 channel 11	Pod A11 channel 11	N-clock
Third time through this procedure		
Pod A2 channel 3	Pod A4 channel 3	J-clock
Pod A6 channel 3	Pod A8 channel 3	L-clock
Pod A10 channel 3	Pod A12 channel 3	N-clock
Fourth time through this procedure		

Pod A2 channel 11	Pod A4 channel 11	J-clock
Pod A6 channel 11	Pod A8 channel 11	L-clock
Pod A10 channel 11	Pod A12 channel 11	N-clock

Connect the 16601A to the Pulse Generator

8133A Ch2 OUTPUT	**8133A Ch2 $\overline{\text{OUTPUT}}$**	**8133A Ch1 OUTPUT**
First time through this procedure		
Pod A1 channel 3	Pod A2 channel 3	J-clock
Pod A3 channel 3	Pod A4 channel 3	L-clock
Pod A5 channel 3	Pod A6 channel 3	N-clock
Pod A7 channel 3	Pod A8 channel 3	
Second time through this procedure		
Pod A1 channel 11	Pod A2 channel 11	J-clock
Pod A3 channel 11	Pod A4 channel 11	L-clock
Pod A5 channel 11	Pod A6 channel 11	N-clock
Pod A7 channel 11	Pod A8 channel 11	

Connect the 16602A to the Pulse Generator

8133A Ch2 OUTPUT	**8133A Ch2 $\overline{\text{OUTPUT}}$**	**8133A Ch1 OUTPUT**
Pod A1 channel 3	Pod A2 channel 3	J-clock
Pod A3 channel 3	Pod A4 channel 3	L-clock
Pod A5 channel 3	Pod A6 channel 3	N-clock
Second time through this procedure		
Pod A1 channel 11	Pod A2 channel 11	J-clock
Pod A3 channel 11	Pod A4 channel 11	L-clock
Pod A5 channel 11	Pod A6 channel 11	N-clock

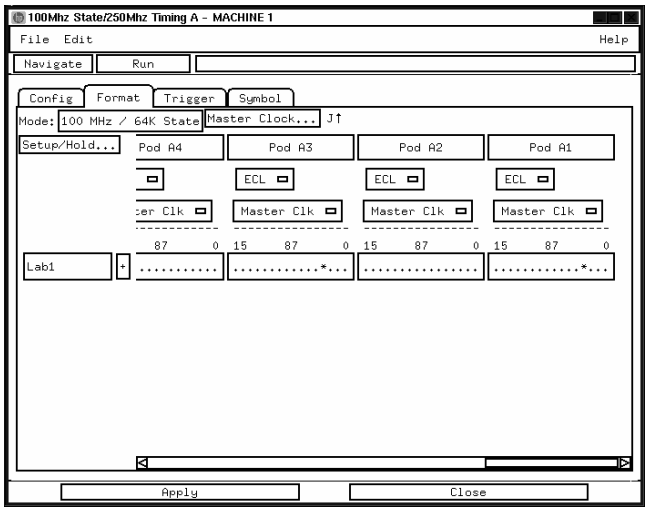
Connect the 16603A to the Pulse Generator

8133A Ch2 OUTPUT	**8133A Ch2 $\overline{\text{OUTPUT}}$**	**8133A Ch1 OUTPUT**
Pod A1 channel 3	Pod A1 channel 11	J-clock
Pod A2 channel 3	Pod A2 channel 11	K-clock
Pod A3 channel 3	Pod A3 channel 11	L-clock
Pod A4 channel 3	Pod A4 channel 11	M-clock

3 Activate the data channels that are connected according to the previous table.

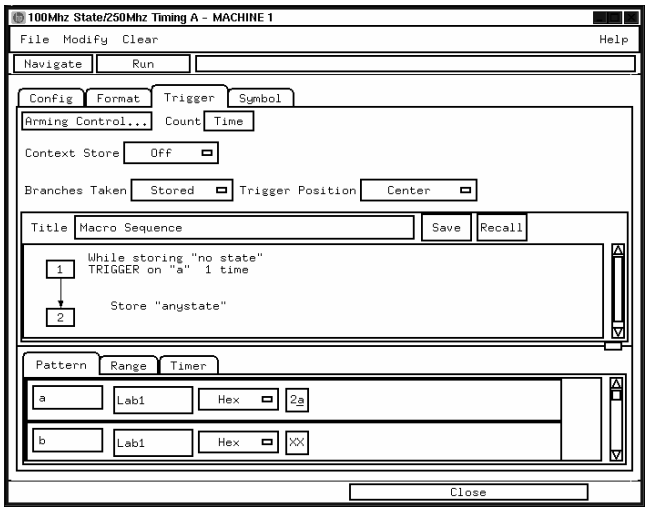
a In the MACHINE 1 setup window, select the Format tab.

b Under the Format tab, select the field showing the channel assignments for one of the pods being tested. Using the mouse, select the data channel to be tested. An asterisk means that a channel is turned on. Follow this step for the remaining pods to be tested.



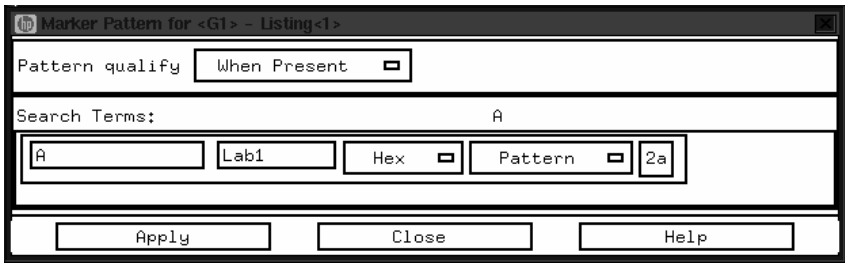
c Under the Trigger tab, select the pattern field associated with pattern recognizer "a". Delete the "XX" and enter the pattern shown below for your analyzer.

Logic Analysis System	Pattern
16600A, 16602A	"2a"
16601A, 16603A	"aa"



d In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window will appear. In the pattern field, enter the value according to the following table. Select Apply, then select Close.

Analyzer	Pattern
16600A, 16602A	"2a"
16601A, 16603A	"aa"



e In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window will appear. In the pattern field, enter the value according to the following table. Select Apply, then select Close.

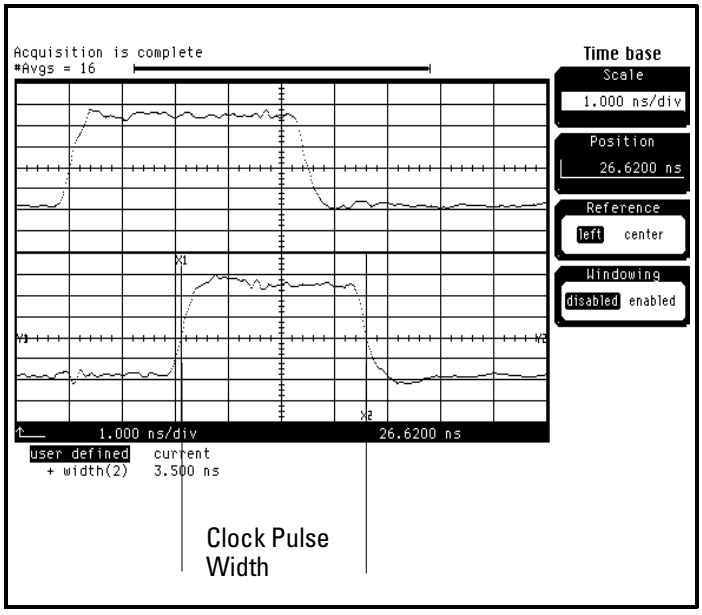
Analyzer	Pattern
16600A, 16602A	"15"
16601A, 16603A	"55"

Verify the test signal

1 Check the clock pulse width. Using the oscilloscope, verify that the clock pulse width is 3.500 ns, +00 ps or -100 ps.

- **a** Enable the pulse generator channel 1, channel 2, AND TRIGGER outputs (LED off).
- **b** In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.
- **c** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that the waveform is centered on the screen.
- **d** On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the clock signal pulse width (+ width (2)).
- **e** If the pulse width is outside the limits, adjust the pulse generator channel 1 width until the pulse width is within limits.

Clock Signal



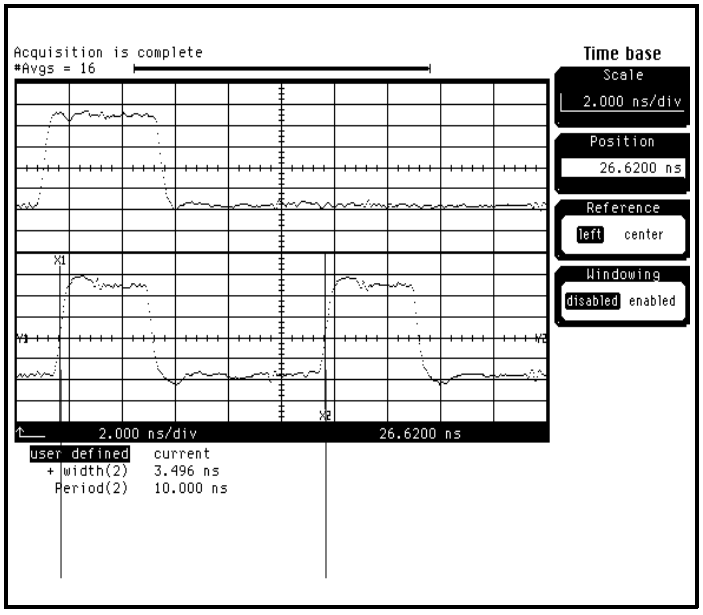
2 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns.

a In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

c On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is not less than 10.000 ns, go to step d. If the period is less than 10.000 ns, go to step 3.

d In the oscilloscope Timebase menu, increase Position 10.000 ns. If the period is not less than 10.000 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than 10.000 ns.



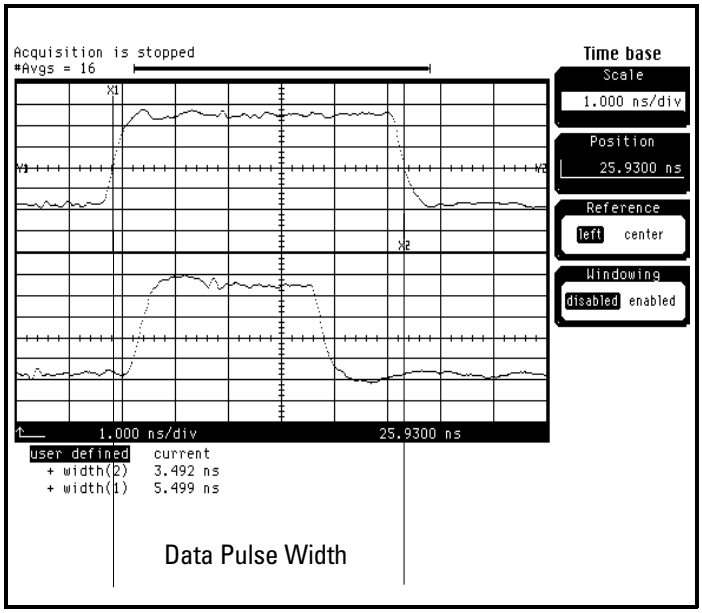
3 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 5.500 ns, +0 ps or - 100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width (1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold with single clock edges, multiple clocks

1 Select the logic analyzer setup/hold time.

a In the MACHINE 1 setup window, select the Format tab.

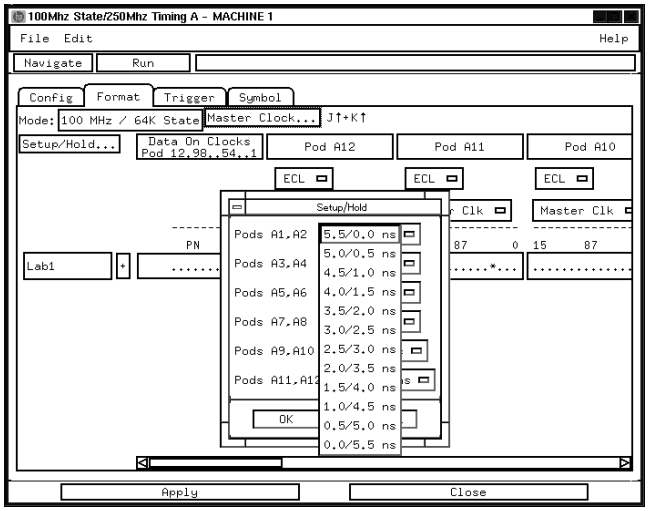
b Under the Format tab, select Master Clock . . . Select and activate any two clock edges, then select Apply.

c Under the Format tab, select Setup/Hold.

d In the Setup/Hold window, select the setup/hold field next to each pod pair, then select the setup/hold combination to be tested. Repeat for all pods.

The first time through this test, select the top combination in the following table.

Setup/Hold Combinations
5.5/0.0 ns
0.0/5.5 ns



d Select OK to exit the Setup/Hold window.

2 Disable the pulse generator channel 1 COMP (LED off).

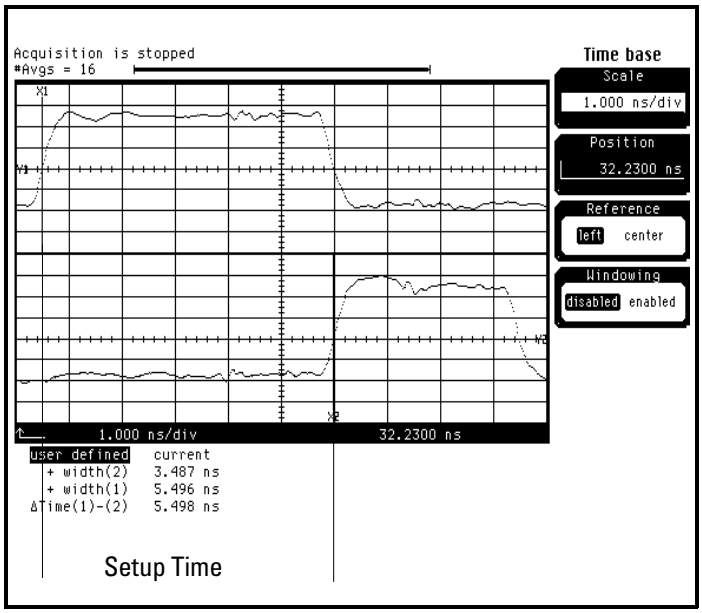
3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the rising edge of the clock waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



4 Select the clock combination to be tested.

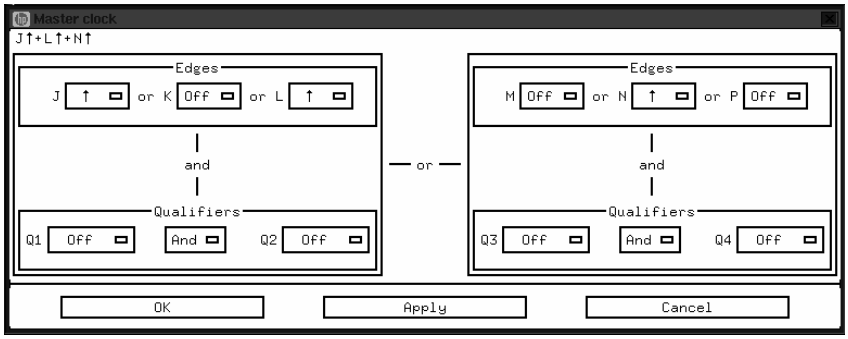
a In the MACHINE 1 setup window under the Format tab, select Master Clock . . .

b In the Master Clock window, select the edge field next to the clock to be tested, then select the clock edge as indicated in the table. Turn off all other clocks.

The first time through this test, select the first clock combination.

Clock Combinations

Analyzer	Clock Combinations	
16600A, 16601A, 16602A	J↑ + L↑ + N↑	K↑ + M↑ + P↑
16603A	J↑ + K↑ + L↑ + M↑	

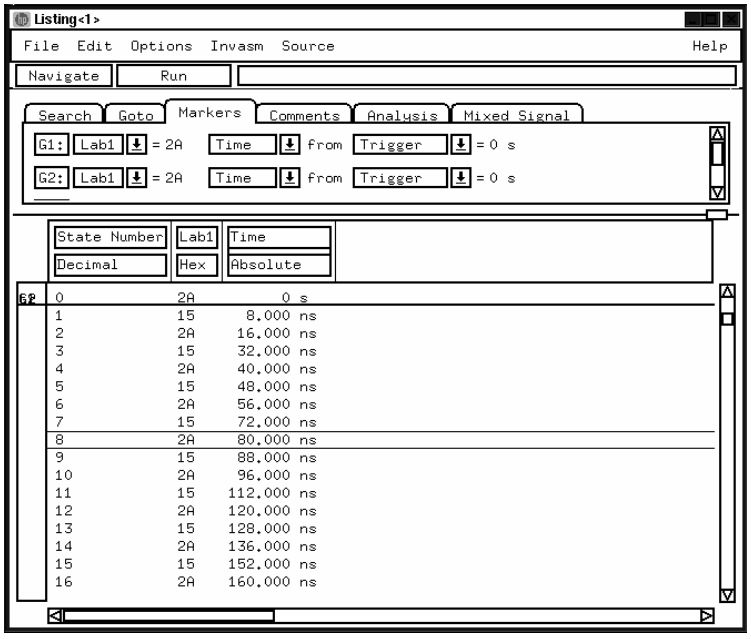


c Select Apply.

d Connect the clock input channels to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

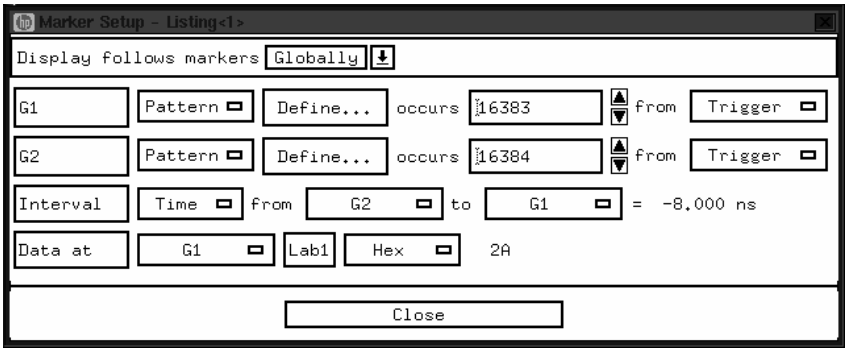
5 Verify the test data.

a In the Listing window, select Run. The display should show an alternating pattern of "2A" and "15" (16600A, 16602A) or "AA" and "55" (16601A, 16603A).



b In the Marker Setup window, select the 'occurs' value field that corresponds to marker G1. Enter 16383.

c In the Marker Setup window, select the 'occurs' value field that corresponds to marker G2. Enter 16384.



d Select Close to apply the marker values to the data. If the "Pattern NOT found for marker..." error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

6 Test the next clock combination (except for 16603A).

a In the MACHINE 1 setup window under the Format tab, select Master Clock . . .

b Repeat steps 4, 5, and 6 for the next clock edge combination listed in the table in step 4, until both clock combinations have been tested.

7 Enable the pulse generator channel 1 COMP (LED on).

8 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: falling.

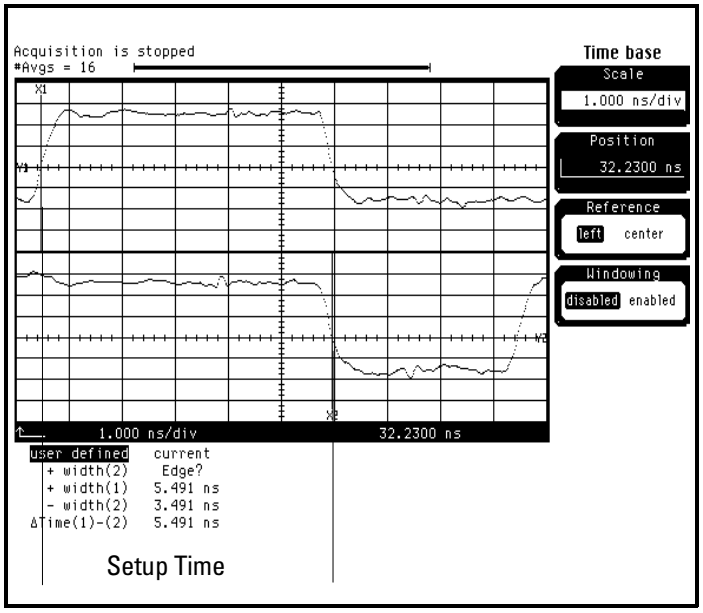
b On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] to verify the clock signal pulse width (- width (2)). If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the clock pulse width is 3.500 ns, +0 ps or -100 ps.

c On the oscilloscope, select [Shift] ΔTime. Select Start src: channel 1, then select [Enter] to display the setup time (ΔTime(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.

Data Signal

Clock Signal



9 Select the clock combination to be tested.

a In the MACHINE 1 setup window under the Format tab, select Master Clock . . .

b In the Master Clock window, select the edge field next to the clocks to be tested, then select the clock edges as indicated in the table. Turn off all other clocks.

The first time through this test, select the first clock combination.

Clock Combinations

Analyzer	Clock Combinations	
16600A, 16601A, 16602A	J↓ + L↓ + N↓	K↓ + M↓ + P↓
16603A	J↓ + K↓ + L↓ + M↓	

c Connect the clock input channel to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

d Select Apply, then select OK to exit the Master Clock menu.

10 Verify the test data.

a In the Listing window, select Run. The display should show an alternating pattern of "2A" and "15" (16600A, 16602A) or "AA" and "55" (16601A, 16603A).

b If the "Pattern NOT found for marker..." error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

11 Test the next clock combination (except for 16603A).

a In the MACHINE 1 setup window under the Format tab, select Master Clock . . .

b Repeat steps 9, 10, and 11 for the next clock combination listed in the table in step 9, until both clock combinations have been tested.

12 If the setup/hold used for the previous steps was 5.5/0.0 ns, repeat steps 1 through 12 using setup/hold 0.0/5.5 ns. If the setup/hold used for the previous steps was 0.0/5.5 ns, continue on with the next section.

Test the next channels (16600A, 16601A, 16602A)

Connect the next combination of data channels and clock channels, and test them.

Starting with "Connect the logic analyzer," connect the next combination, then continue through the complete test. Repeat until all data channel combinations have been tested.

To Test the Single-clock, Multiple-edge, State Acquisition

Testing the single-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time

This test checks a combination of data channels using a multiple-edge single clock at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, <600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, <58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)		8120-4948
Coupler (Qty 3)	BNC(m-m)	1250-0216
BNC Test Connector, 6x2 (Qty 3)		

Set up the equipment

1 If you have not already done so, do the procedure "To Set up the Test Equipment and the Analyzer". Use the pulse generator settings listed below.

2 Set up the pulse generator according to the following table.

Timebase	Channel 2	Trigger	Channel 1
Mode: Int Period: 20.000 ns	Mode: Pulse Divide: PULSE ÷ 1 Width: 5.000 ns	Divide: Divide ÷ 1 Ampl: 0.50 V Offs: 0.00 V	Mode: Square Delay: 0.000 ns

Set up the logic analyzer

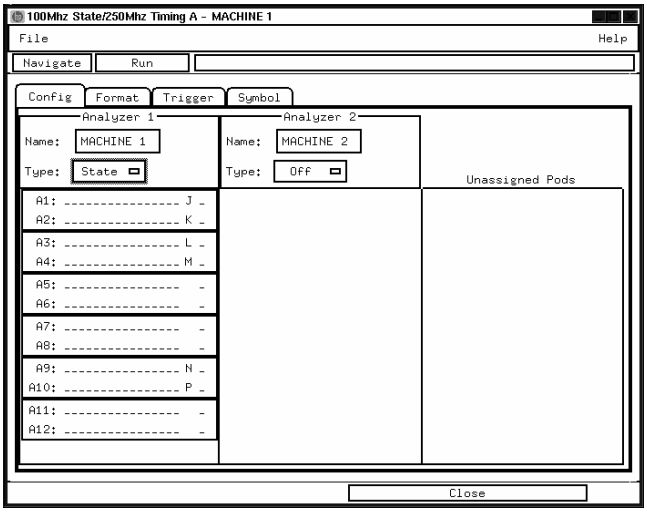
Perform the following steps if you have not done so for the previous tests.

1 Set up the Configuration window.

a In the MACHINE 1 window, select the Config tab.

b In the Analyzer 1 Type box select Timing, then in the pop-up menu select State.

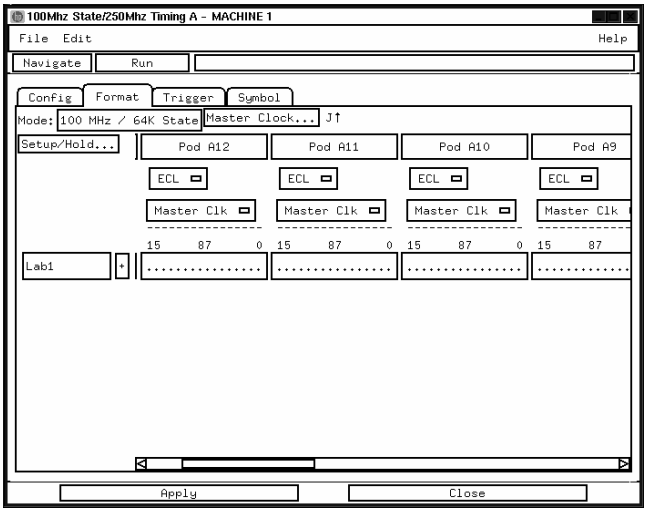
2 Under the Config tab, assign all pods to Analyzer 1. To assign the pods, use the mouse to drag the pods to the Analyzer 1 column.



3 Set up the Format window.

a In the MACHINE 1 setup window, select the Format tab.

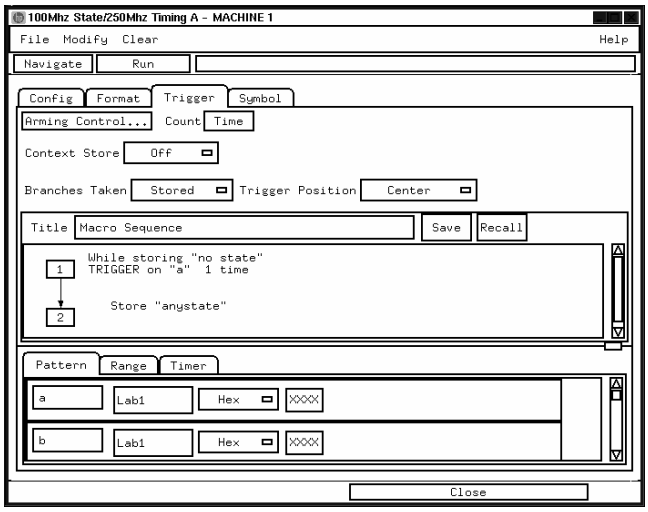
b Under each Pod field, select TTL, then select ECL. The screen does not show all pod fields at one time. To access more pod fields, use the scroll bars of the MACHINE 1 window.



4 Set up the Trigger window.

a In the MACHINE 1 setup window, select the Trigger tab. Under the Trigger tab, select the Pattern tab at the bottom of the window.

b Click and hold the field labeled "1" in the Sequence field, then slide the cursor to Edit and release the mouse. In the pop-up window, select "anystate", then select "no state". Select Close.

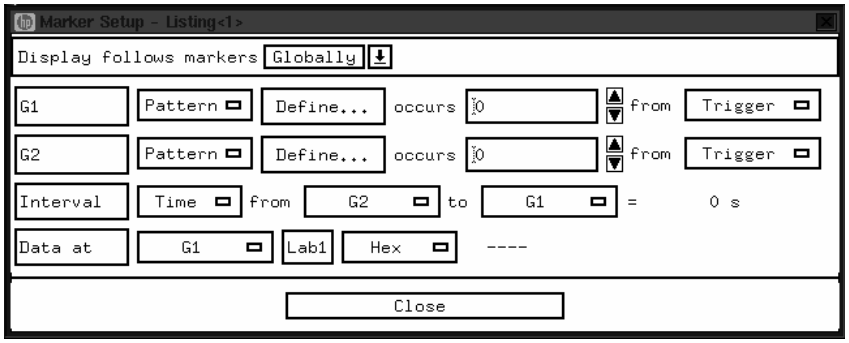


5 Set up the Listing window.

a In the Listing window, select the Markers tab.

b Select the G1: field and the Markers Setup window will appear.

c Select the Sample field associated with G1, and select Pattern. Select the Sample field associated with G2, and select Pattern.

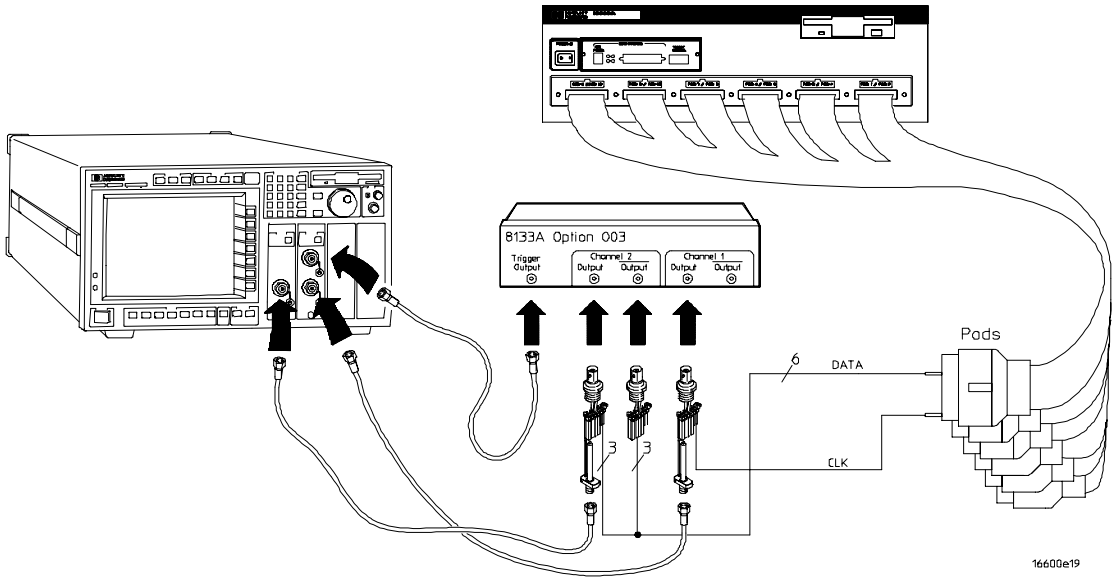


Note: Leave the Marker Setup window open. You will be entering numeric values in the "occurs" field after acquiring the test data.

Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following tables to the pulse generator. Note that this procedure is repeated several times for this test, and each time you use a different set of channels. There is also a different set of tables for each 16600-series logic analysis system.

2 Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator according to the following illustration. Use the data and clock according to the table for your logic analysis system.



Connect the 16600A to the Pulse Generator

8133A Ch2 OUTPUT	8133A Ch2 $\overline{\text{OUTPUT}}$	8133A Ch1 OUTPUT
First time through this procedure		
Pod A1 channel 3 Pod A5 channel 3 Pod A9 channel 3	Pod A3 channel 3 Pod A7 channel 3 Pod A11 channel 3	J-clock
Second time through this procedure		
Pod A1 channel 11 Pod A5 channel 11 Pod A9 channel 11	Pod A3 channel 11 Pod A7 channel 11 Pod A11 channel 11	J-clock
Third time through this procedure		
Pod A2 channel 3 Pod A6 channel 3 Pod A10 channel 3	Pod A4 channel 3 Pod A8 channel 3 Pod A12 channel 3	J-clock
Fourth time through this procedure		
Pod A2 channel 11 Pod A6 channel 11 Pod A10 channel 11	Pod A4 channel 11 Pod A8 channel 11 Pod A12 channel 11	J-clock

Connect the 16601A to the Pulse Generator

8133A Ch2 OUTPUT	8133A Ch2 $\overline{\text{OUTPUT}}$	8133A Ch1 OUTPUT
First time through this procedure		
Pod A1 channel 3	Pod A2 channel 3	J-clock
Pod A3 channel 3	Pod A4 channel 3	
Pod A5 channel 3	Pod A6 channel 3	
Pod A7 channel 3	Pod A8 channel 3	
Second time through this procedure		
Pod A1 channel 11	Pod A2 channel 11	J-clock
Pod A3 channel 11	Pod A4 channel 11	
Pod A5 channel 11	Pod A6 channel 11	
Pod A7 channel 11	Pod A8 channel 11	

Connect the 16602A to the Pulse Generator

8133A Ch2 OUTPUT	8133A Ch2 $\overline{\text{OUTPUT}}$	8133A Ch1 OUTPUT
First time through this procedure		
Pod A1 channel 3	Pod A2 channel 3	J-clock
Pod A3 channel 3	Pod A4 channel 3	
Pod A5 channel 3	Pod A6 channel 3	
Second time through this procedure		
Pod A1 channel 11	Pod A2 channel 11	J-clock
Pod A3 channel 11	Pod A4 channel 11	
Pod A5 channel 11	Pod A6 channel 11	

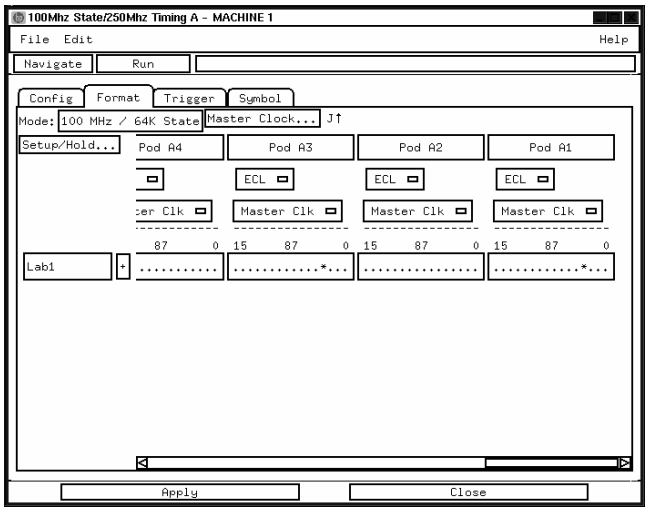
Connect the 16603A to the Pulse Generator

8133A Ch2 OUTPUT	8133A Ch2 $\overline{\text{OUTPUT}}$	8133A Ch1 OUTPUT
Pod A1 channel 3	Pod A1 channel 11	J-clock
Pod A2 channel 3	Pod A2 channel 11	
Pod A3 channel 3	Pod A3 channel 11	
Pod A4 channel 3	Pod A4 channel 11	

3 Activate the data channels that are connected according to the previous table.

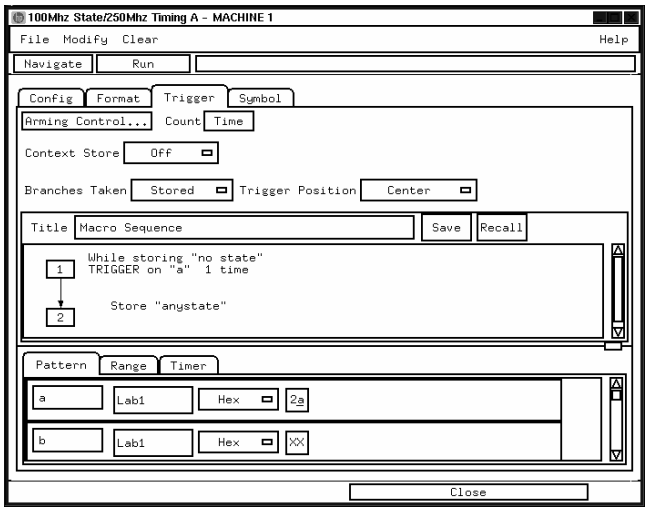
a In the MACHINE 1 setup window, select the Format tab.

b Under the Format tab, select the field showing the channel assignments for one of the pods being tested. Using the mouse, select the data channel to be tested. An asterisk means that a channel is turned on. Follow this step for the remaining pods to be tested.



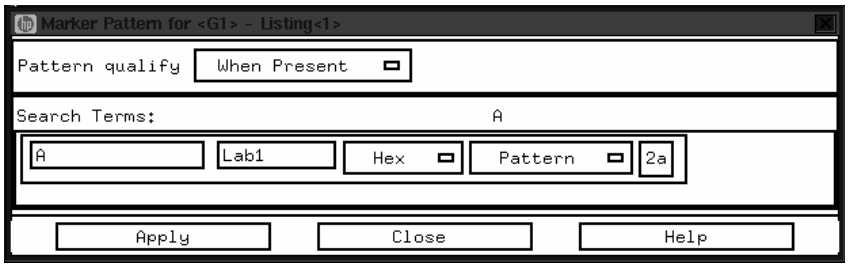
c Under the Trigger tab, select the pattern field associated with pattern recognizer "a". Delete the "XX" and enter the pattern shown below for your analyzer.

Logic Analysis System	Pattern
16600A, 16602A	"2a"
16601A, 16603A	"aa"



d In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window will appear. In the pattern field, enter the value according to the following table. Select Apply, then select Close.

Analyzer	Pattern
16600A, 16602A	"2a"
16601A, 16603A	"aa"



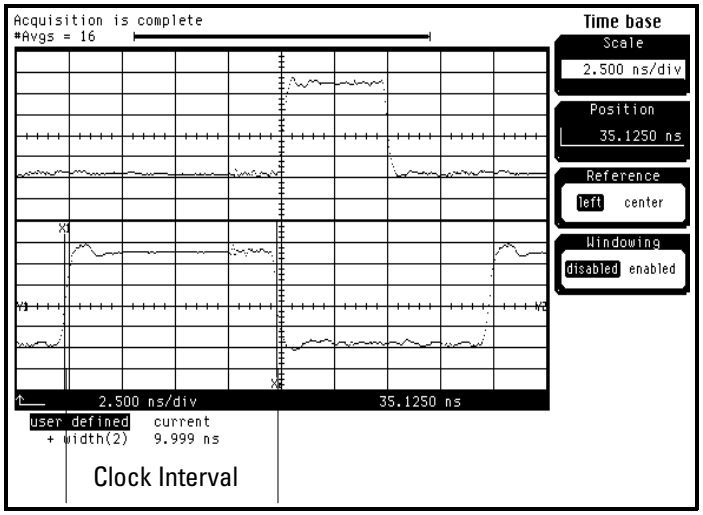
e In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window will appear. In the pattern field, enter the value according to the following table. Select Apply, then select Close.

Analyzer	Pattern
16600A, 16602A	"15"
16601A, 16603A	"55"

Verify the test signal

1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or -250 ps.

- **a** In the oscilloscope Timebase menu, select Scale: 2.500 ns/div.
- **b** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.
- **c** On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the master-to-master clock time (+ width(2)). If the positive-going pulse width is more than 10.000 ns, go to step d. If the positive-going pulse width is less than or equal to 10.000 ns but greater than 9.750 ns, go to step 2.
- **d** On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] (- width(2)). If the negative pulse width is less than or equal to 10.000 ns but greater than 9.750 ns, go to step 2.
- **e** Decrease the pulse generator Period in 10 ps increments until the oscilloscope + width (2) or - width (2) read less than or equal to 10.000 ns, but greater than 9.750 ns.



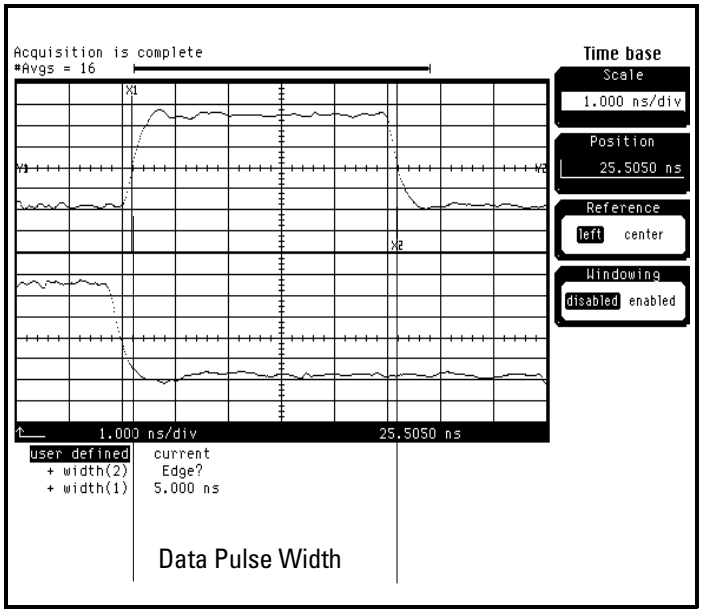
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 5.000 ns, +0 ps or -100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold with single clock, multiple clock edges

1 Select the logic analyzer setup/hold time.

a In the MACHINE 1 setup window under the Format tab, select Master Clock . . .

b In the Master Clock window, activate a rising and falling edge for any clock.

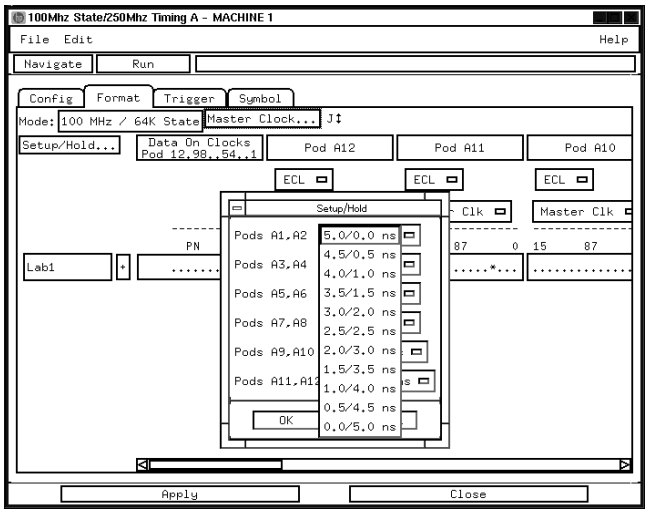
The Setup/Hold window requires a double clock edge before it will allow a setup/hold of 5.0/0.0 ns.

c Under the Format tab, select Setup/Hold.

d In the Setup/Hold window, select the setup/hold field next to each pod pair, then select the setup/hold combination to be tested. Repeat for all pods.

The first time through this test, select the top combination in the following table.

Setup/Hold Combinations
5.0/0.0 ns
0.0/5.0 ns



d Select OK to exit the Setup/Hold window.

2 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

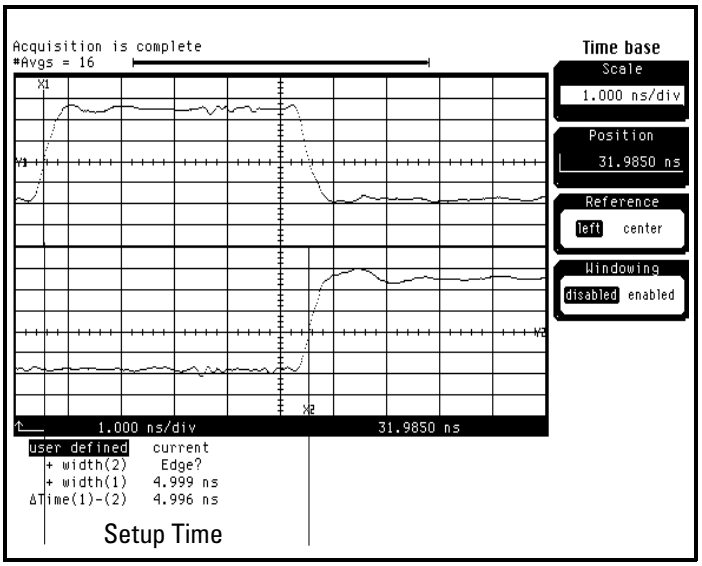
b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the falling edge of the data waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 2 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.

Data Signal

Clock Signal



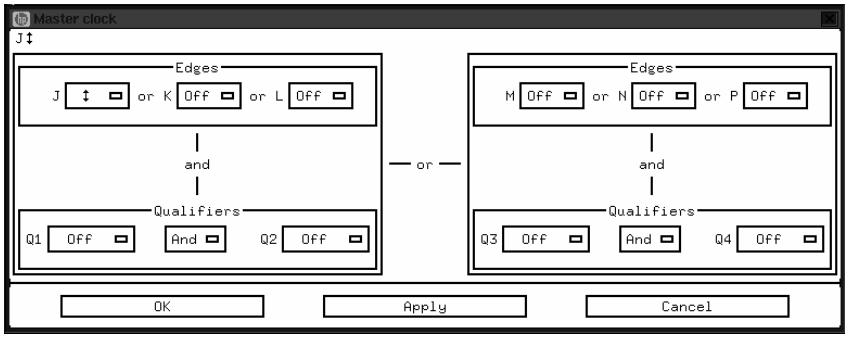
3 Select the clock to be tested.

a In the MACHINE 1 setup window under the Format tab, select Master Clock . . .

b In the Master Clock window, select the edge field next to the clock to be tested, then select the clock edge as indicated in the table. Ensure all other clocks are turned off.

The first time through this test, select the first clock and edge.

Analyzer	Clocks					
16600A, 16601A, 16602A	J↕	K↕	L↕	M↕	N↕	P↕
16603A	J↕	K↕	L↕	M↕		

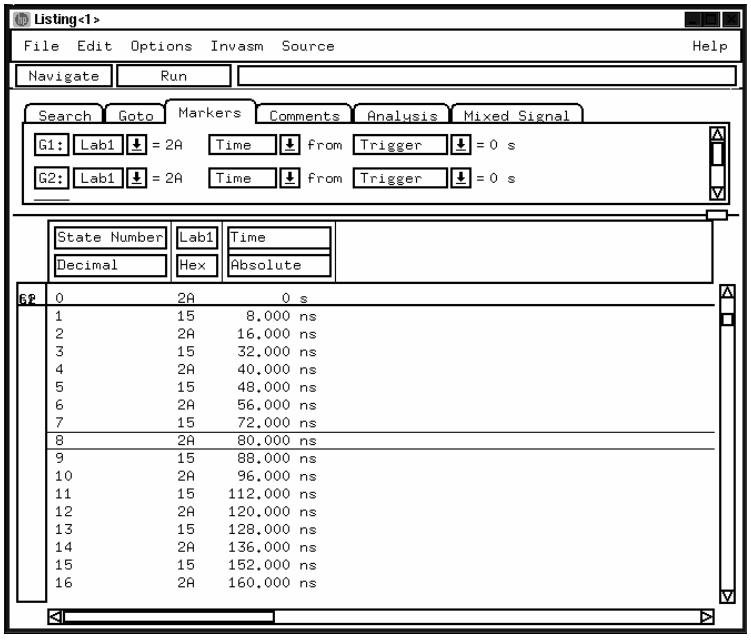


c Connect the clock input channel to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

d Select Apply, then select OK to exit the Master Clock menu.

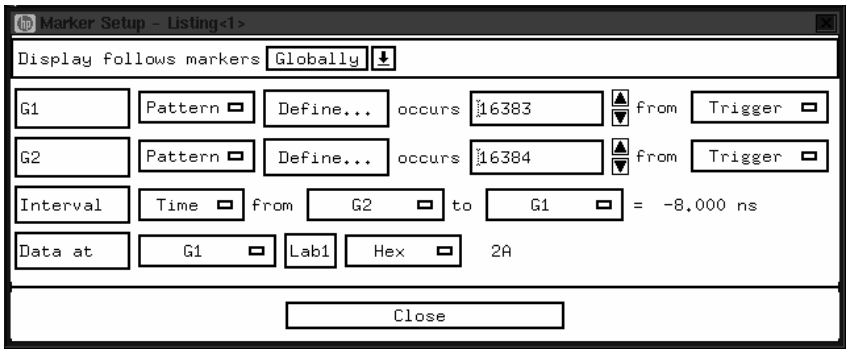
4 Verify the test data.

a In the Listing window, select Run. The display should show an alternating pattern of "2A" and "15" (16600A, 16602A) or "AA" and "55" (16601A, 16603A).



b In the Marker Setup window, select the 'occurs' value field that corresponds to marker G1. Enter 16383.

c In the Marker Setup window, select the 'occurs' value field that corresponds to marker G2. Enter 16384.



d Select Close to apply the marker values to the data. If the "Pattern NOT found for marker..." error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

5 Test the next clock.

a In the MACHINE 1 setup window under the Format tab, select Master Clock . . .

b Repeat steps 3, 4, and 5 for the next clock edge listed in the table in step 3, until all listed clock edges have been tested.

6 If the setup/hold used for the previous steps was 5.0/0.0 ns, repeat steps 1 through 5 using setup/hold 0.0/5.0 ns. If the setup/hold used for the previous steps was 0.0/5.0 ns, continue on with the next section.

Test the next channels (16600A, 16601A, 16602A)

Connect the next combination of data channels and clock channels, and test them.

Starting with "Connect the logic analyzer," connect the next combination, then continue through the complete test. Repeat until all data channel combinations have been tested.

To Test the Time Interval Accuracy

Testing the time interval accuracy does not check a specification, but does check the following:

- 125 MHz oscillator

This test verifies that the 125 MHz timing acquisition synchronizing oscillator is operating within limits.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Pulse Generator	100 MHz, 3.5 ns pulse width, <600 ps rise time	8133A Option 003
Function Generator	Accuracy $\leq (5)(10^{-6}) \times$ frequency	8656B Option 002
SMA Coax Cable	18 GHz Bandwidth	8120-4948
BNC cable		8120-1840
Adapter	SMA(m)-BNC(f)	1250-1200
Adapter	BNC(m)-SMA(f)	1250-2015
Coupler	BNC(m-m)	1250-0216
BNC Test Connector, 6x2		

Set up the equipment

1 If you have not already done so, do the procedure "To set up the test equipment and the logic analyzer".

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Trigger
Mode: Ext Period: 25.000 ns	Mode: Square Delay: 0.000 ns High: -0.90 V Low: -1.70 V COMP: Disabled (LED Off)	Divide: Divide ÷ 1 Ampl: 0.50 V Offs: 0.00 V

3 Set up the high frequency function generator according to the following table.

Function Generator Setup

Freq: 40.000 00 MHz

Amptd: 1.00 V

Modulation: Off

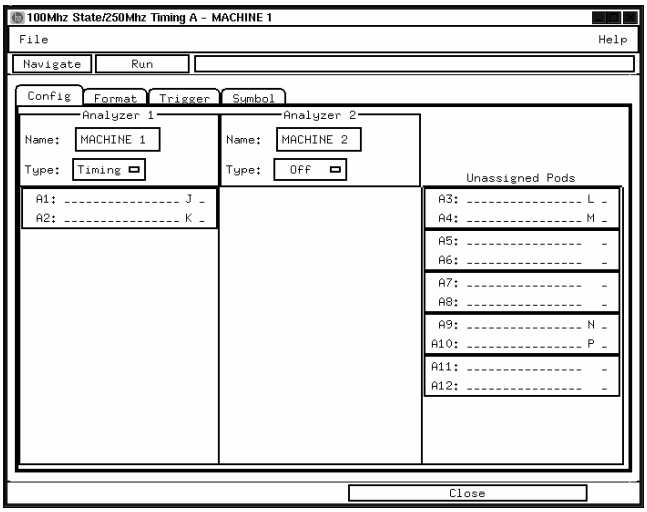
Set up the logic analyzer

1 Set up the Configuration menu.

a In the MACHINE 1 window, select the Config tab.

b In the Analyzer 1 box, select State, then in the pop-up menu select Timing.

c Unassign all pods from Analyzer 1 except for Pod A1 and A2. To deassign the remaining pods, drag and drop the pods to the Unassigned Pods column using the mouse. Only Pods A1 and A2 should remain assigned to Analyzer 1.

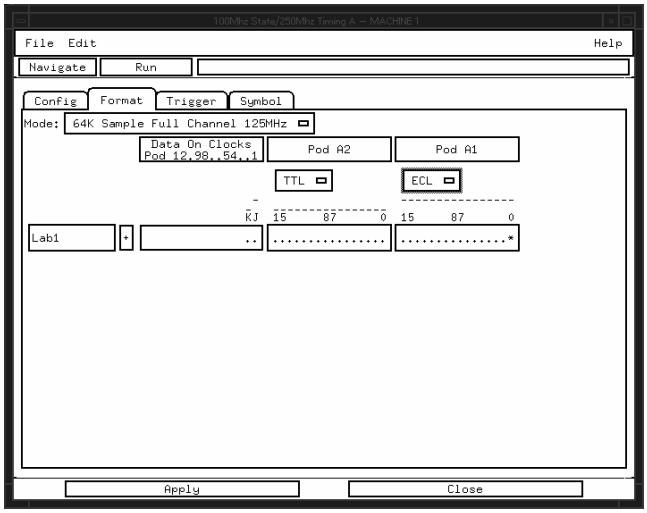


2 Set up the Format menu.

a In the MACHINE 1 setup window, select the Format tab.

b Under the Pod A1 field, select TTL, then select ECL.

c Under the Format tab, select the field showing the channel assignments for Pod A1. Using the mouse, first clear the channels (all "."), then select channel 1. An asterisk means that the channel is turned on.

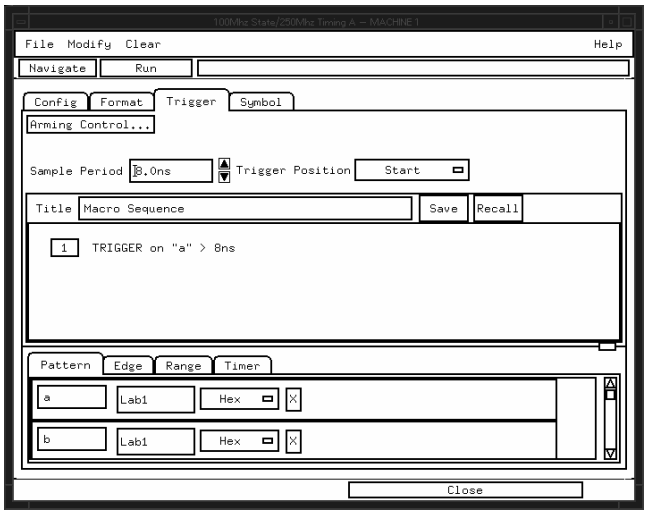


3 Set up the Trigger menu.

a In the MACHINE 1 setup window, select the Trigger tab. Select Clear, then select All.

b Under the Trigger tab, select Trigger Position, then select Start.

c Select the sample period value field, then enter 8.0.



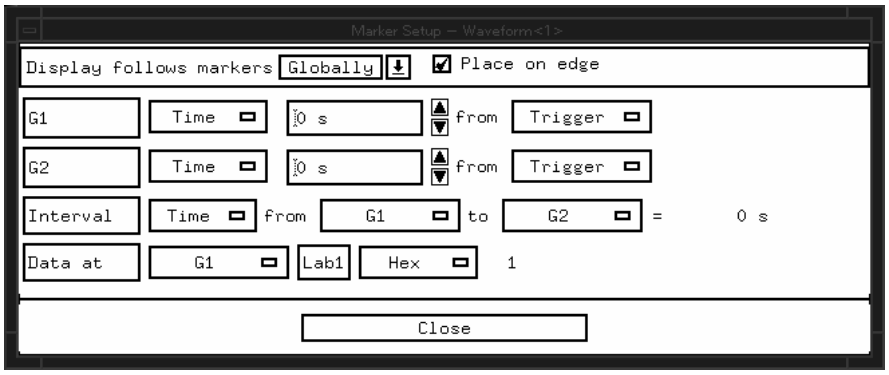
4 Set up the Waveform menu.

a In the MACHINE 1 window, select Navigate, then select Slot A: MACHINE 1, then select Waveform. A Waveform window will now open.

b In the Waveform window select the Markers tab.

c Select the G1 field and a Marker Setup window will appear.

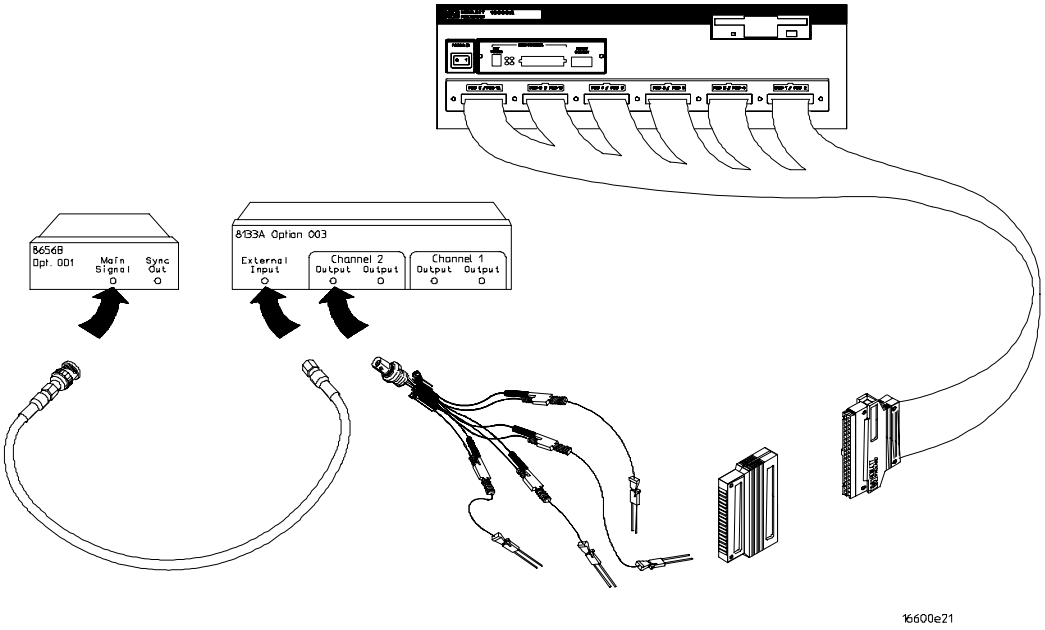
c Ensure that the Interval Time field reads "from G1 to G2" (instead of "from G2 to G1").



Leave this window open as you will be using it later when acquiring data.

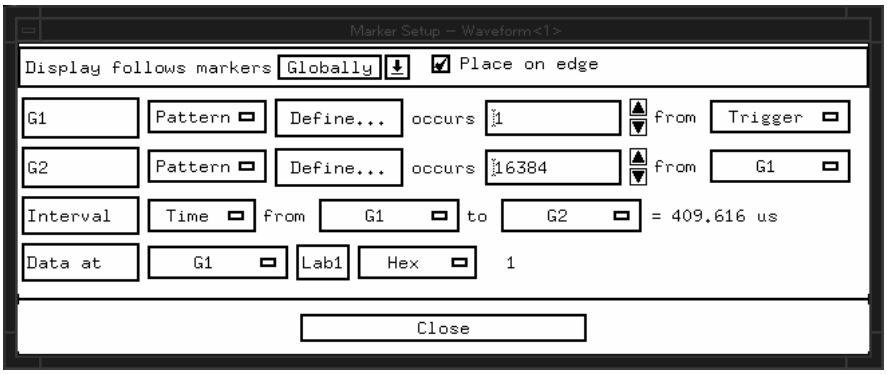
Connect the logic analyzer

1 Using a 6-by-2 test connector, connect channel 0 of Pod A1 to the pulse generator channel 2 output.
2 Using the SMA cable and the BNC adapter, connect the External Input of the pulse generator to the Main Signal of the function generator.



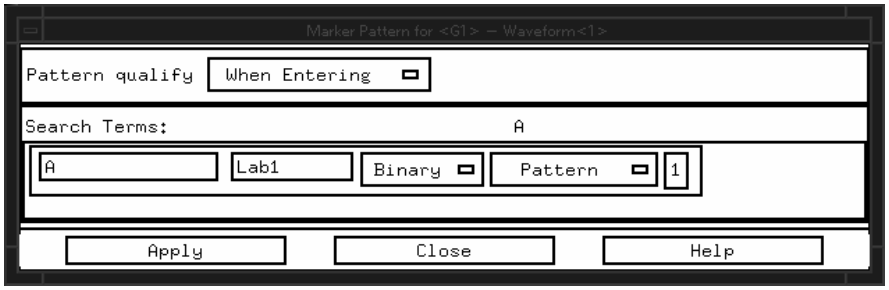
Acquire the data

1 Enable the pulse generator channel 2 and trigger outputs (with the LED off).
2 In the logic analyzer Waveform menu, select Run.
3 Configure the Markers to measure the time interval.
   a In the Marker Setup window select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select pattern.
   b Select the Occurs field associated with G1 and enter "1". Select the Occurs field associated with G2 and enter "16384".
   c Select the From field associated with G2 and select G1.



In the Marker Setup window, you will observe the Interval Time from G1 to G2 = value to determine the pass or fail status of this test.

d In the marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window will appear. In the Pattern field, enter "1". Select the Pattern Qualify field and select When Entering. Select Apply, then select Close.



e In the marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window will appear. In the Pattern field, enter "1". Select the Pattern Qualify field and select When Entering. Select Apply, then select Close.

4 Acquire the data.

a In the Waveform menu, move the mouse cursor over Run and click and hold the right mouse button. At the pop-up menu, select Repetitive.

b Select Run. The logic analyzer will now repetitively acquire data.

c Continuously observe the Interval Time from G1 to G2 = value in the Marker Setup window.

Allow the logic analyzer to run repetitively for approximately one minute. If the Interval Time value remains inside the range 409.552 µs to 409.648 µs, the test passes. Record a Pass or Fail in the performance test record.

d Select Stop to end the acquisition.

Performance Test Record

	16600-series Logic Analysis System_____
Serial No._____	Work Order No._____
Recommended Test Interval - 2 Year/4000 hours	Date_____
Recommended next testing_____	Temperature_____

Test	**Settings**		**Results**	
Self-Tests	Board Verification Tests Acquisition IC Verification Tests		Pass/Fail Pass/Fail	_____ _____
Threshold Accuracy	± (100 mV + 3% of threshold setting)			
			Limits	Measured
Pod A1	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod A2	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod A3	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod A4	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod A5	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod A6	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod A7	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____

Performance Test Record (continued)

Test	Settings		Results			
Threshold Accuracy (continued)			Limits	Measured		
Pod A8	ECL, ±139 mV	ECL VL	-1.439 V	_____		
		ECL VH	-1.161 V	_____		
	0 V, ±100 mV	0 V User VL	-100 mV	_____		
		0 V User VH	+100 mV	_____		
Pod A9	ECL, ±139 mV	ECL VL	-1.439 V	_____		
		ECL VH	-1.161 V	_____		
	0 V, ±100 mV	0 V User VL	-100 mV	_____		
		0 V User VH	+100 mV	_____		
Pod A10	ECL, ±139 mV	ECL VL	-1.439 V	_____		
		ECL VH	-1.161 V	_____		
	0 V, ±100 mV	0 V User VL	-100 mV	_____		
		0 V User VH	+100 mV	_____		
Pod A11	ECL, ±139 mV	ECL VL	-1.439 V	_____		
		ECL VH	-1.161 V	_____		
	0 V, ±100 mV	0 V User VL	-100 mV	_____		
		0 V User VH	+100 mV	_____		
Pod A12	ECL, ±139 mV	ECL VL	-1.439 V	_____		
		ECL VH	-1.161 V	_____		
	0 V, ±100 mV	0 V User VL	-100 mV	_____		
		0 V User VH	+100 mV	_____		
Single-Clock, Single-Edge Acquisition			Disable pulse generator, channel 1 COMP (LED off)		Enable pulse generator, channel 1 COMP (LED on)	
16600				**Pass/Fail**		**Pass/Fail**
Pods A1, A3, A5, A7, A9, A11, channel 3	Setup/Hold Time	4.5/0.0 ns	J↑	_____	J↓	_____
			K↑	_____	K↓	_____
			L↑	_____	L↓	_____
			M↑	_____	M↓	_____
			N↑	_____	N↓	_____
			P↑	_____	P↓	_____
Pods A1, A3, A5, A7, A9, A11, channel 11	Setup/Hold Time	4.5/0.0 ns	J↑	_____	J↓	_____
			K↑	_____	K↓	_____
			L↑	_____	L↓	_____
			M↑	_____	M↓	_____
			N↑	_____	N↓	_____
			P↑	_____	P↓	_____
Pods A2, A4, A6, A8, A10, A12, channel 3	Setup/Hold Time	4.5/0.0 ns	J↑	_____	J↓	_____
			K↑	_____	K↓	_____
			L↑	_____	L↓	_____
			M↑	_____	M↓	_____
			N↑	_____	N↓	_____
			P↑	_____	P↓	_____

Test	Settings		Results			
Single-Clock, Single-Edge Acquisition (continued)			Disable pulse generator, channel 1 COMP (LED off)		Enable pulse generator, channel 1 COMP (LED on)	
Pods A2, A4, A6, A8, A10, A12, channel 11	Setup/Hold Time	4.5/0.0 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
Pods A1, A3, A5, A7, A9, A11, channel 3	Setup/Hold Time	0.0/4.5 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
Pods A1, A3, A5, A7, A9, A11, channel 11	Setup/Hold Time	0.0/4.5 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
Pods A2, A4, A6, A8, A10, A12, channel 3	Setup/Hold Time	0.0/4.5 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
Pods A2, A4, A6, A8, A10, A12, channel 11	Setup/Hold Time	0.0/4.5 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
16601/02						
All pods, channel 3	Setup/Hold Time	4.5/0.0 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
All pods, channel 11	Setup/Hold Time	4.5/0.0 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
All pods, channel 3	Setup/Hold Time	0.0/4.5 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____

Test	Settings		Results			
Single-Clock, Single-Edge Acquisition (continued)			Disable pulse generator, channel 1 COMP (LED off)		Enable pulse generator, channel 1 COMP (LED on)	
All pods, channel 11	Setup/Hold Time	0.0/4.5 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
16603						
All pods, channels 3 and 11	Setup/Hold Time	0.0/4.5 ns	J↑ K↑ L↑ M↑	_____ _____ _____ _____	J↓ K↓ L↓ M↓	_____ _____ _____ _____
All pods, channels 3 and 11	Setup/Hold Time	0.0/4.5 ns	J↑ K↑ L↑ M↑	_____ _____ _____ _____	J↓ K↓ L↓ M↓	_____ _____ _____ _____
Multiple-Clock, Multiple-Edge Acquisition			Disable pulse generator, channel 1 COMP (LED off)		Enable pulse generator, channel 1 COMP (LED on)	
16600				**Pass/Fail**		**Pass/Fail**
Pods A1, A3, A5, A7, A9, A11, channel 3	Setup/Hold Time	5.5/0.0 ns	J↑ + L↑ + N↑	_____	J↓ + L↓ + N↓	_____
Pods A1, A3, A5, A7, A9, A11, channel 11	Setup/Hold Time	5.5/0.0 ns	J↑ + L↑ + N↑	_____	J↓ + L↓ + N↓	_____
Pods A2, A4, A6, A8, A10, A12, channel 3	Setup/Hold Time	5.5/0.0 ns	J↑ + L↑ + N↑	_____	J↓ + L↓ + N↓	_____
Pods A2, A4, A6, A8, A10, A12, channel 11	Setup/Hold Time	5.5/0.0 ns	J↑ + L↑ + N↑	_____	J↓ + L↓ + N↓	_____
Pods A1, A3, A5, A7, A9, A11, channel 3	Setup/Hold Time	5.5/0.0 ns	K↑ + M↑ + P↑	_____	K↓ + M↓ + P↓	_____
Pods A1, A3, A5, A7, A9, A11, channel 11	Setup/Hold Time	5.5/0.0 ns	K↑ + M↑ + P↑	_____	K↓ + M↓ + P↓	_____
Pods A2, A4, A6, A8, A10, A12, channel 3	Setup/Hold Time	5.5/0.0 ns	K↑ + M↑ + P↑	_____	K↓ + M↓ + P↓	_____
Pods A2, A4, A6, A8, A10, A12, channel 11	Setup/Hold Time	5.5/0.0 ns	K↑ + M↑ + P↑	_____	K↓ + M↓ + P↓	_____

Test	Settings		Results			
Multiple-Clock, Multiple-Edge Acquisition (continued)			Disable pulse generator, channel 1 COMP (LED off)		Enable pulse generator, channel 1 COMP (LED on)	
16600				**Pass/Fail**		**Pass/Fail**
Pods A1, A3, A5, A7, A9, A11, channel 3	Setup/Hold Time	0.0/5.5 ns	J↑ + L↑ + N↑	_____	J↓ + L↓ + N↓	_____
Pods A1, A3, A5, A7, A9, A11, channel 11	Setup/Hold Time	0.0/5.5 ns	J↑ + L↑ + N↑	_____	J↓ + L↓ + N↓	_____
Pods A2, A4, A6, A8, A10, A12, channel 3	Setup/Hold Time	0.0/5.5 ns	J↑ + L↑ + N↑	_____	J↓ + L↓ + N↓	_____
Pods A2, A4, A6, A8, A10, A12, channel 11	Setup/Hold Time	0.0/5.5 ns	J↑ + L↑ + N↑	_____	J↓ + L↓ + N↓	_____
Pods A1, A3, A5, A7, A9, A11, channel 3	Setup/Hold Time	0.0/5.5 ns	K↑ + M↑ + P↑	_____	K↓ + M↓ + P↓	_____
Pods A1, A3, A5, A7, A9, A11, channel 11	Setup/Hold Time	0.0/5.5 ns	K↑ + M↑ + P↑	_____	K↓ + M↓ + P↓	_____
Pods A2, A4, A6, A8, A10, A12, channel 3	Setup/Hold Time	0.0/5.5 ns	K↑ + M↑ + P↑	_____	K↓ + M↓ + P↓	_____
Pods A2, A4, A6, A8, A10, A12, channel 11	Setup/Hold Time	0.0/5.5 ns	K↑ + M↑ + P↑	_____	K↓ + M↓ + P↓	_____
16601/02				**Pass/Fail**		**Pass/Fail**
All pods, channel 3	Setup/Hold Time	5.5/0.0 ns	J↑ + L↑ + N↑	_____	J↓ + L↓ + N↓	_____
All pods, channel 11	Setup/Hold Time	5.5/0.0 ns	J↑ + L↑ + N↑	_____	J↓ + L↓ + N↓	_____
All pods, channel 3	Setup/Hold Time	5.5/0.0 ns	K↑ + M↑ + P↑	_____	K↓ + M↓ + P↓	_____
All pods, channel 11	Setup/Hold Time	5.5/0.0 ns	K↑ + M↑ + P↑	_____	K↓ + M↓ + P↓	_____
All pods, channel 3	Setup/Hold Time	0.0/5.5 ns	J↑ + L↑ + N↑	_____	J↓ + L↓ + N↓	_____
All pods, channel 11	Setup/Hold Time	0.0/5.5 ns	J↑ + L↑ + N↑	_____	J↓ + L↓ + N↓	_____
All pods, channel 3	Setup/Hold Time	0.0/5.5 ns	K↑ + M↑ + P↑	_____	K↓ + M↓ + P↓	_____
All pods, channel 11	Setup/Hold Time	0.0/5.5 ns	K↑ + M↑ + P↑	_____	K↓ + M↓ + P↓	_____

Test	Settings		Results			
Multiple-Clock, Multiple-Edge Acquisition (continued)			Disable pulse generator, channel 1 COMP (LED off)		Enable pulse generator, channel 1 COMP (LED on)	
16603				**Pass/Fail**		**Pass/Fail**
All pods, channels 3 and 11	Setup/Hold Time	5.5/0.0 ns	J↑ + K↑ + L↑ + M↑	_____	J↓ + K↓ + L↓ + M↓	_____
All pods, channels 3 and 11	Setup/Hold Time	0.0/5.5 ns	J↑ + K↑ + L↑ + M↑	_____	J↓ + K↓ + L↓ + M↓	_____
Single-Clock, Multiple-Edge Acquisition						
16600						**Pass/Fail**
Pods A1, A3, A5, A7, A9, A11, channel 3	Setup/Hold Time	5.0/0.0 ns	J↕ K↕ L↕ M↕ N↕ P↕			_____ _____ _____ _____ _____ _____
Pods A1, A3, A5, A7, A9, A11, channel 11	Setup/Hold Time	5.0/0.0 ns	J↕ K↕ L↕ M↕ N↕ P↕			_____ _____ _____ _____ _____ _____
Pods A2, A4, A6, A8, A10, A12, channel 3	Setup/Hold Time	5.0/0.0 ns	J↕ K↕ L↕ M↕ N↕ P↕			_____ _____ _____ _____ _____ _____
Pods A2, A4, A6, A8, A10, A12, channel 11	Setup/Hold Time	5.0/0.0 ns	J↕ K↕ L↕ M↕ N↕ P↕			_____ _____ _____ _____ _____ _____
Pods A1, A3, A5, A7, A9, A11, channel 3	Setup/Hold Time	0.0/5.0 ns	J↕ K↕ L↕ M↕ N↕ P↕			_____ _____ _____ _____ _____ _____
Pods A1, A3, A5, A7, A9, A11, channel 11	Setup/Hold Time	0.0/5.0 ns	J↕ K↕ L↕ M↕ N↕ P↕			_____ _____ _____ _____ _____ _____

Test	Settings		Results	
Single-Clock, Multiple-Edge Acquisition (continued)				
Pods A2, A4, A6, A8, A10, A12, channel 3	Setup/Hold Time	0.0/5.0 ns	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____
Pods A2, A4, A6, A8, A10, A12, channel 11	Setup/Hold Time	0.0/5.0 ns	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____
16601/02				Pass/Fail
All pods, channel 3	Setup/Hold Time	5.0/0.0 ns	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____
All pods, channel 11	Setup/Hold Time	5.0/0.0 ns	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____
All pods, channel 3	Setup/Hold Time	0.0/5.0 ns	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____
All pods, channel 11	Setup/Hold Time	0.0/5.0 ns	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____
16603				Pass/Fail
All pods, channels 3 and 11	Setup/Hold Time	0.0/5.0 ns	J↕ K↕ L↕ M↕	_____ _____ _____ _____
All pods, channels 3 and 11	Setup/Hold Time	0.0/5.0 ns	J↕ K↕ L↕ M↕	_____ _____ _____ _____

Test	Settings	Results Pass/Fail
Time Interval Accuracy		
	Interval time from G1 to G2 409.552 - 409.648 µs	_____

4

Calibrating and Adjusting

Calibrating and Adjusting

This chapter normally gives you instructions for calibrating and adjusting the logic analysis system.

The 16600A-series mainframe does not require adjustments.

Calibrations and Adjustments for Modules

The 16600A-series Logic Analysis System does not require an operational accuracy calibration. To test the instrument against specifications, refer to "Testing Performance" in chapter 3.

The individual measurement modules that can plug into the 16600A-series Logic Analysis System may require calibration, operational accuracy calibration, or adjustments. Refer to the appropriate documentation for the individual modules for recommended calibration and operational accuracy calibration intervals and procedures, and adjustment procedures.

5

Troubleshooting

Troubleshooting

This chapter helps you troubleshoot the logic analysis system to find defective assemblies. The troubleshooting consists of flowcharts, self-test instructions, and tests. This information is not intended for component-level repair.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform other tests. The other tests are located in this chapter after the flowcharts.

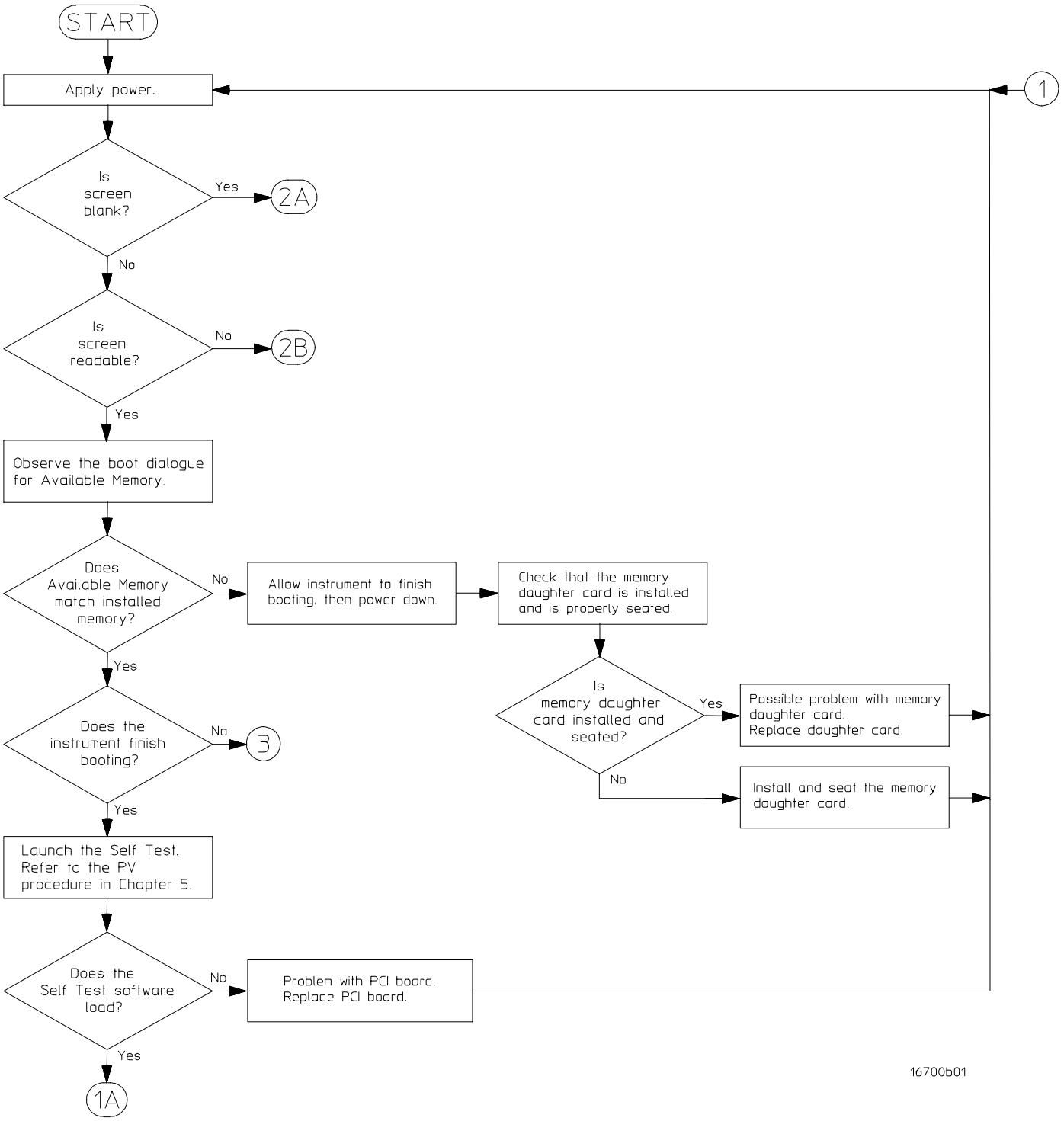
The service strategy for this instrument is the replacement of defective assemblies. This instrument can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

CAUTION

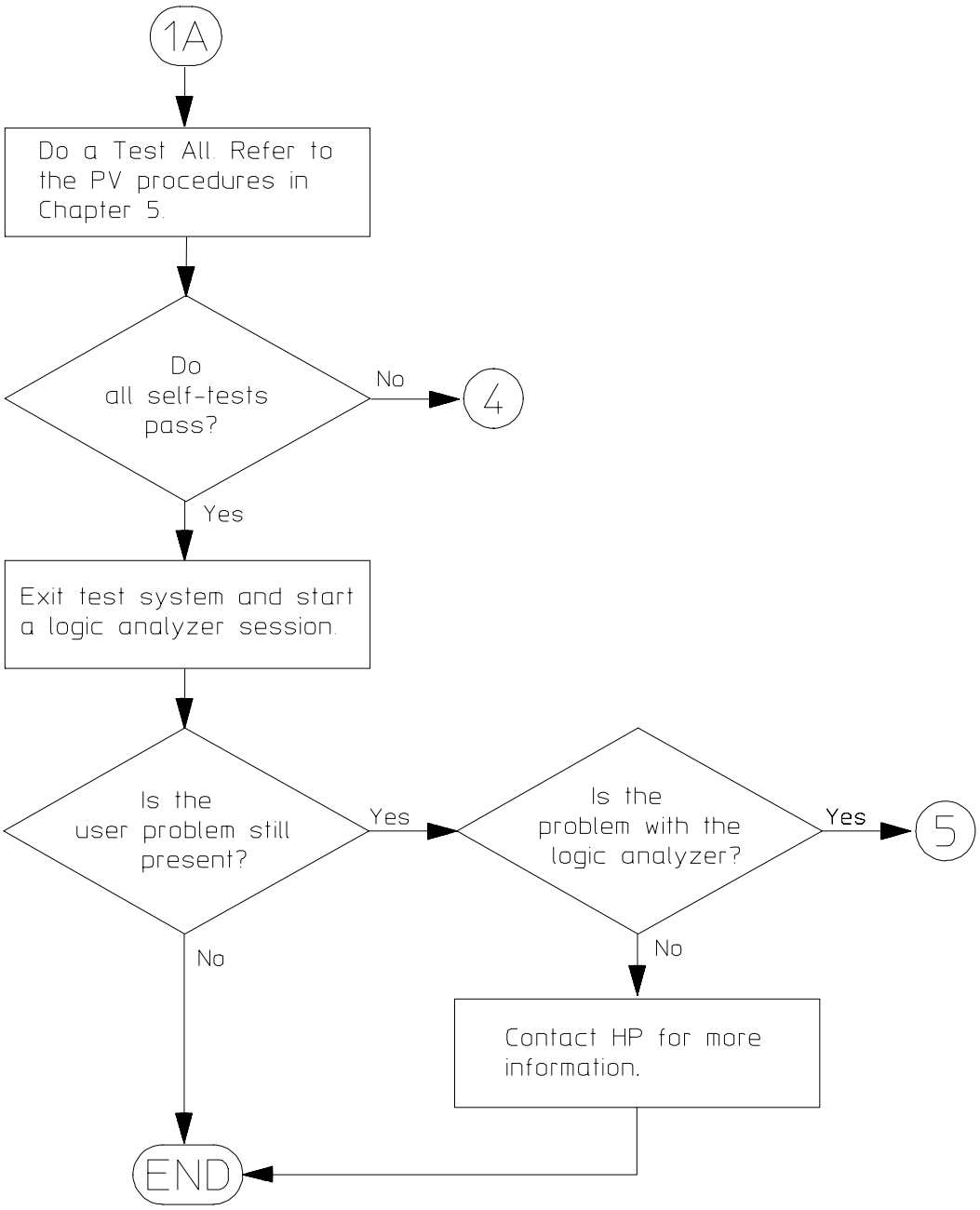
Electrostatic discharge can damage electronic components. Use grounded wrist straps and mats when you perform any service to this instrument or to the cards in it.

To use the flowcharts

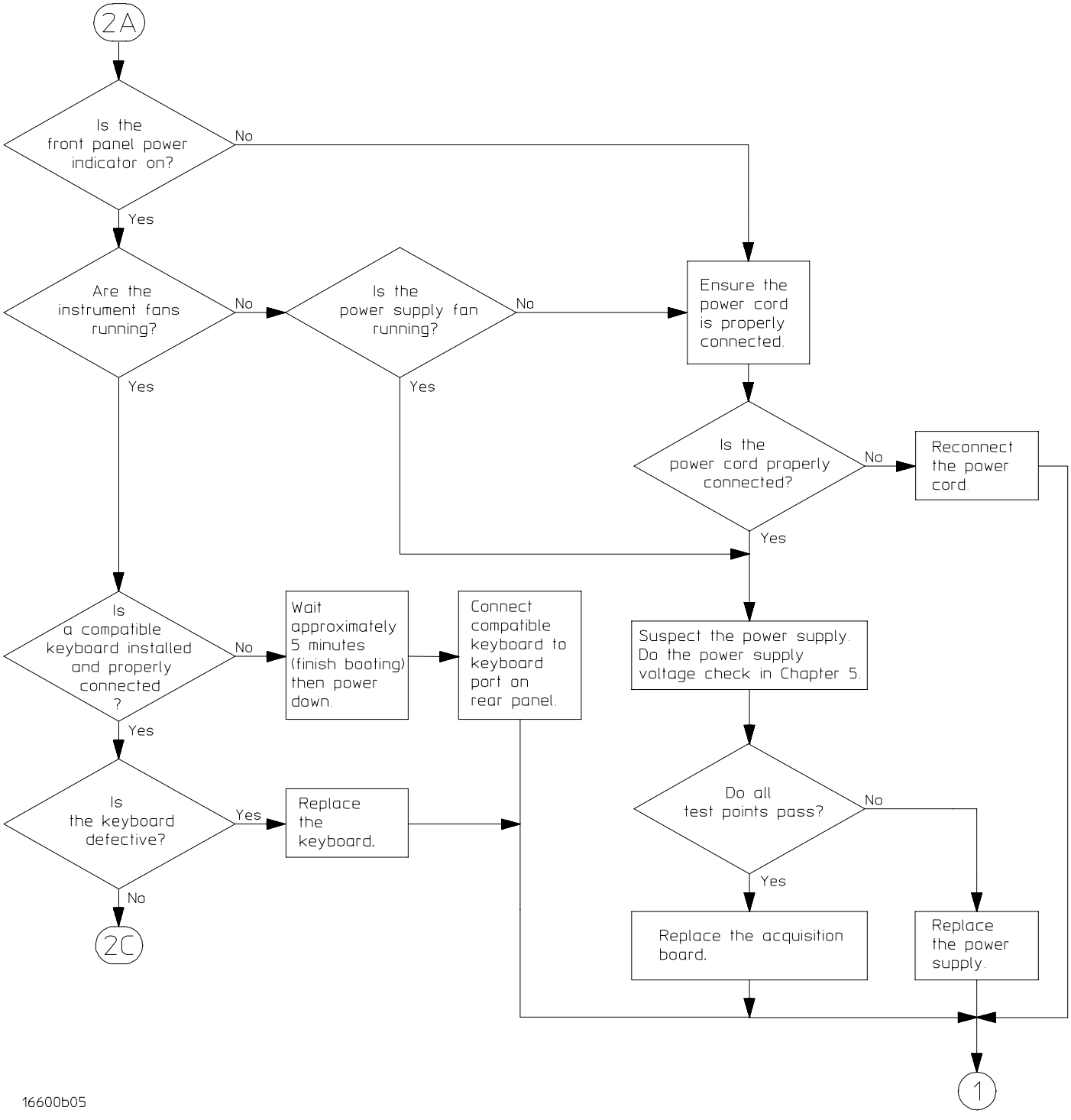
Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled letters on the charts indicate connections with the other flowcharts. Start your troubleshooting at the top of the first flowchart.



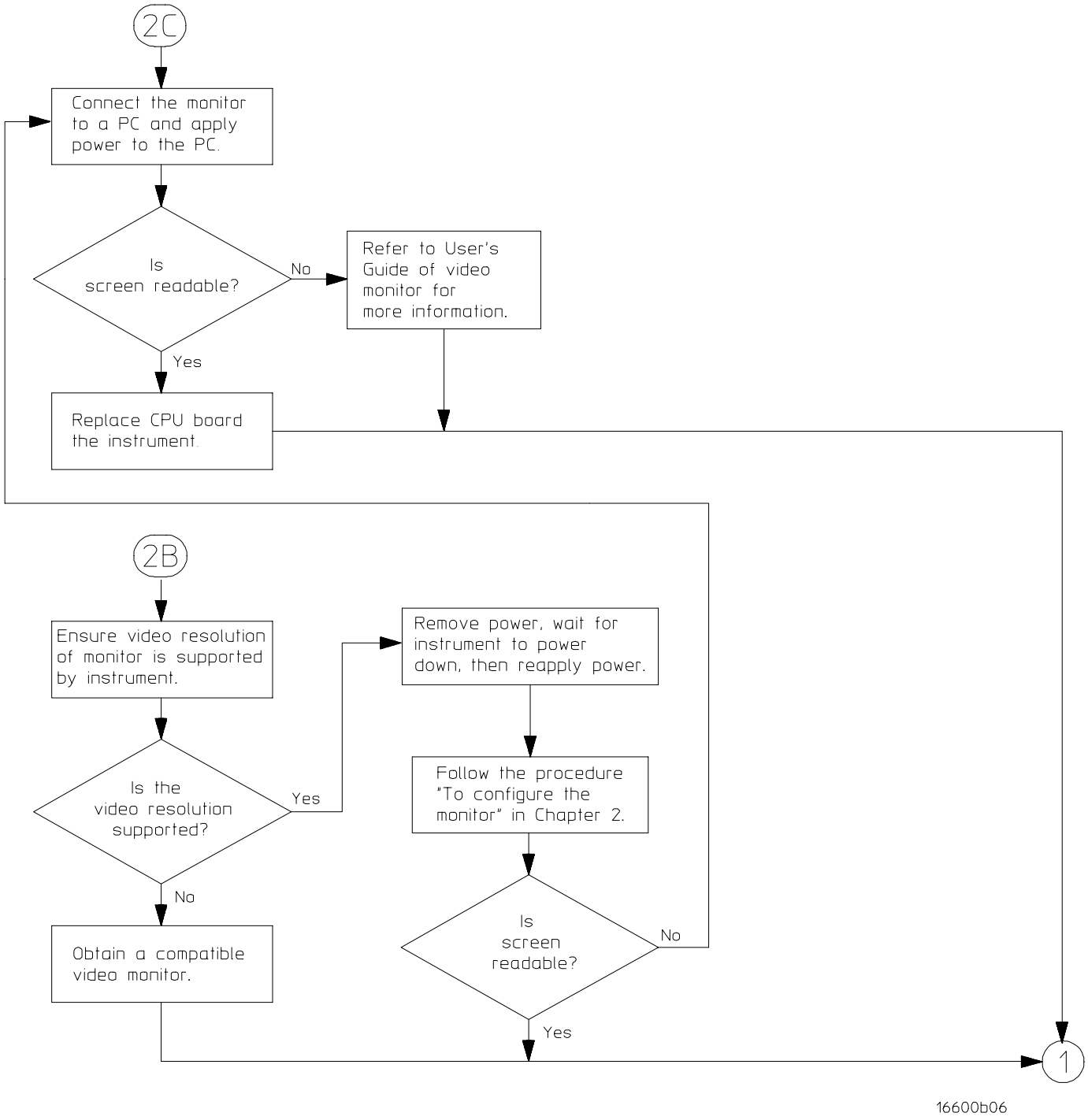
Troubleshooting Flowchart



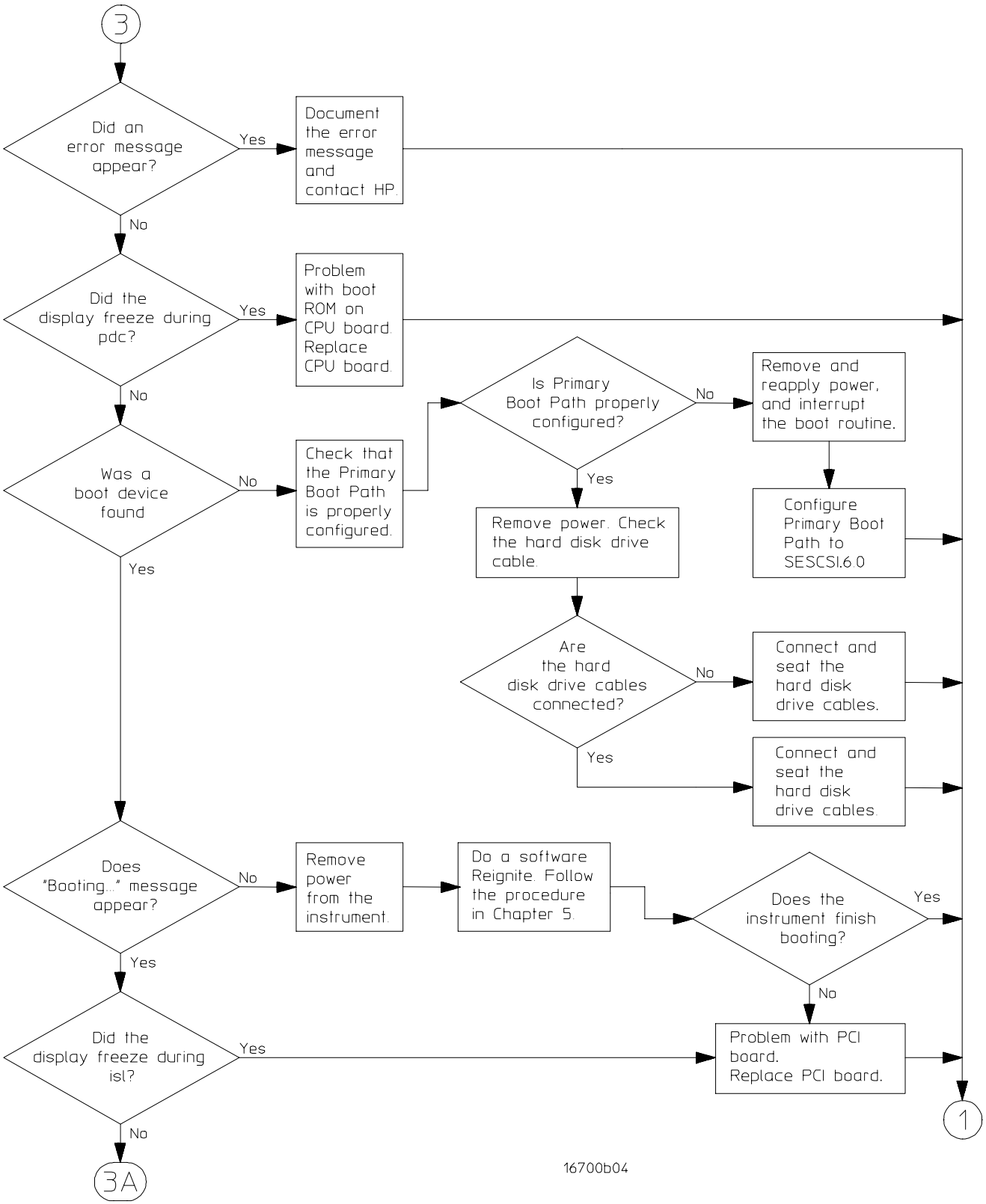
Troubleshooting Flowchart



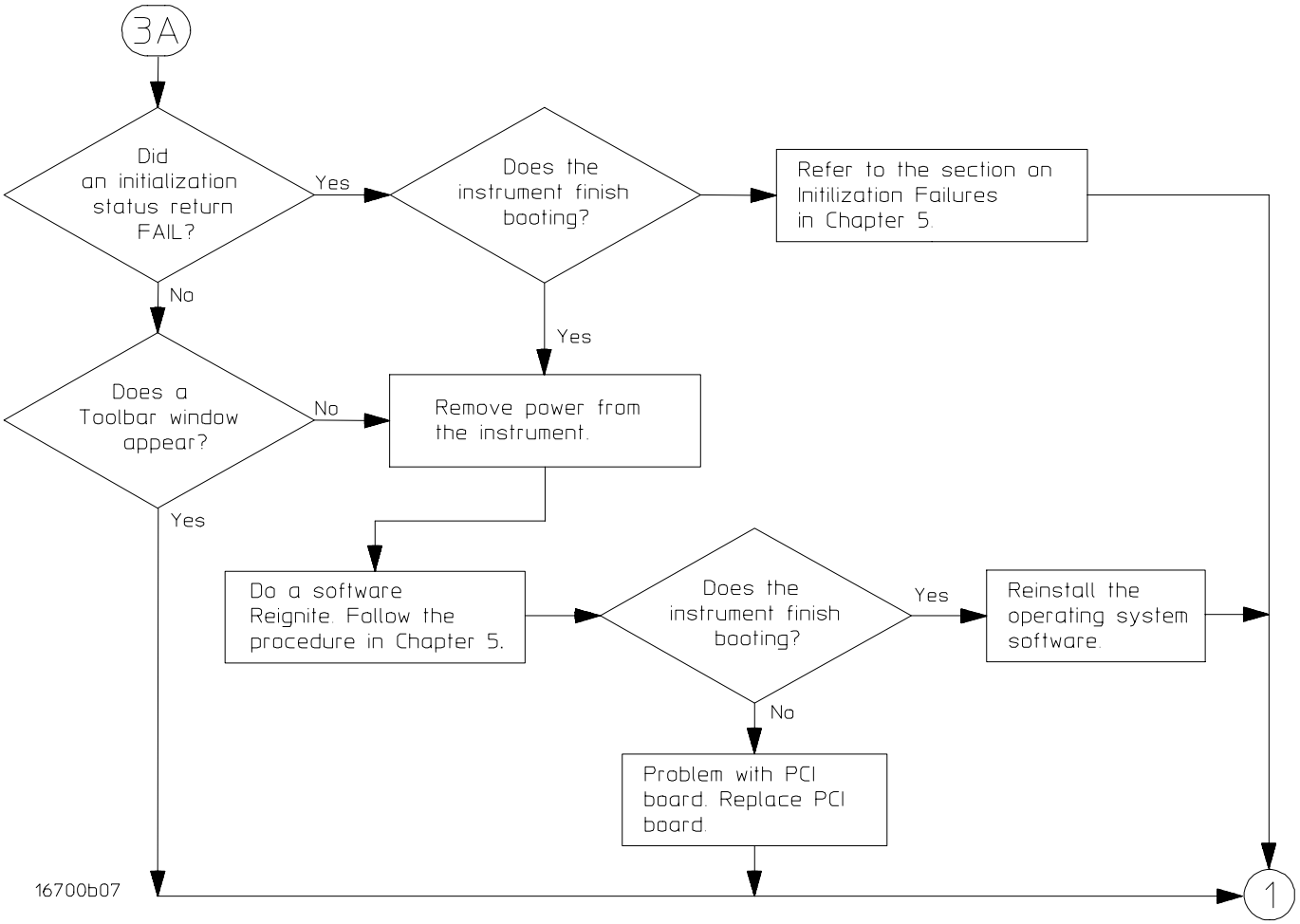
Troubleshooting Flowchart



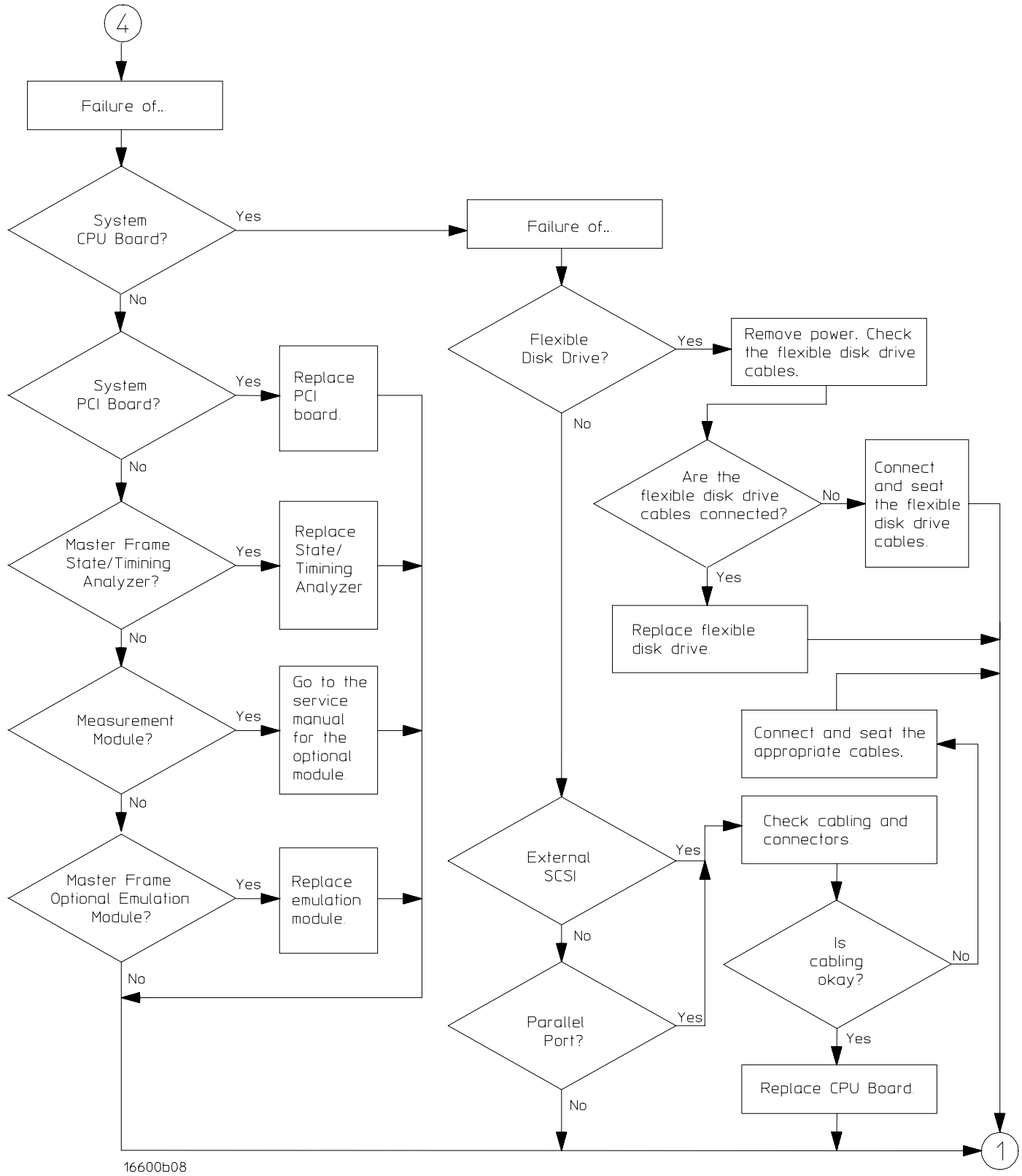
Troubleshooting Flowchart



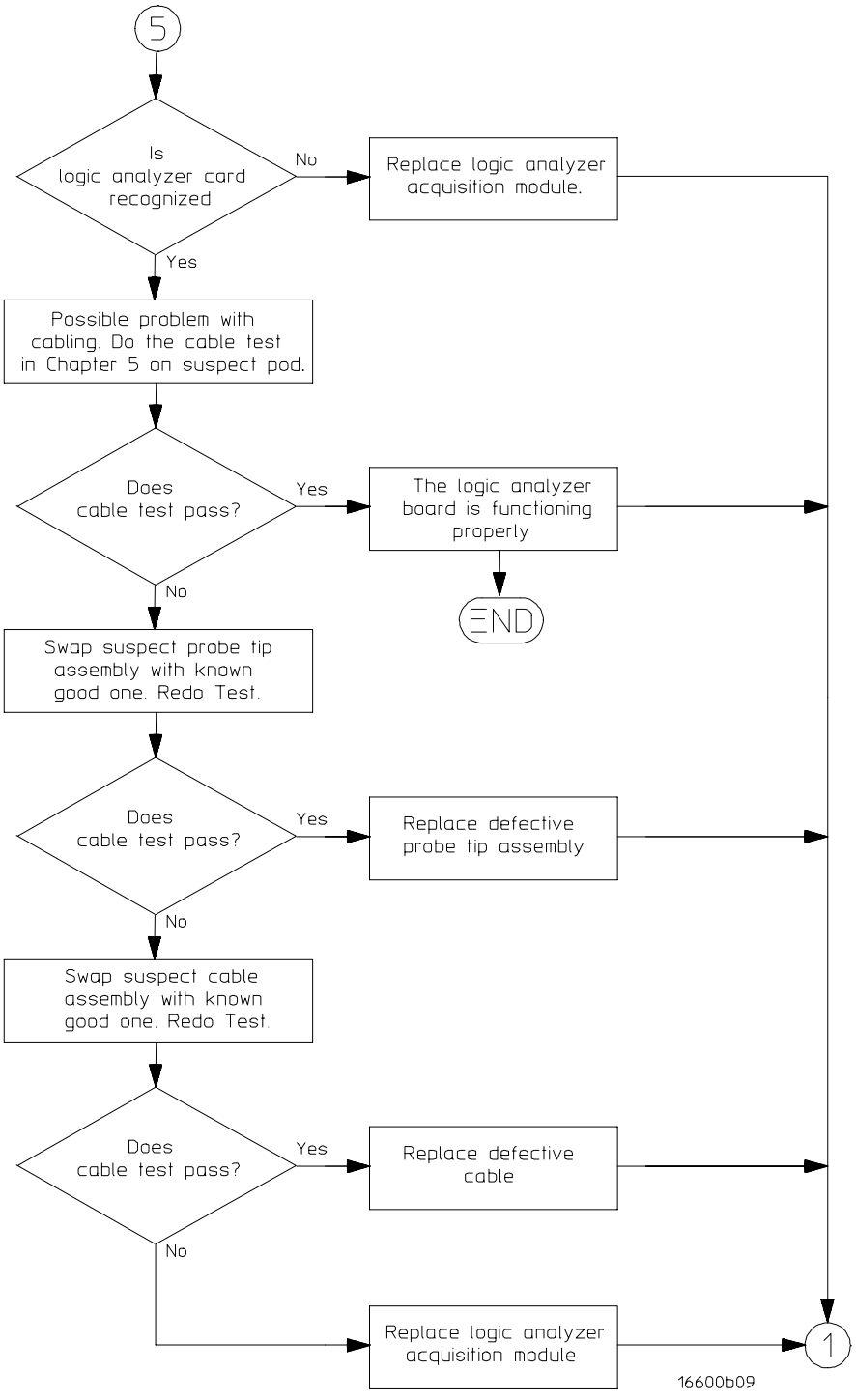
Troubleshooting Flowchart



Troubleshooting Flowchart



Troubleshooting Flowchart



Troubleshooting Flowchart

To perform the power-up tests

The logic analysis system automatically performs power-up tests when you apply power to the instrument. Any errors are reported in the boot dialogue. Serious errors will interrupt the boot process.

The power-up tests are designed to complement the instrument on-line Self Tests. Tests that are performed during power-up are not repeated in the Self Tests.

The monitor, keyboard and mouse must be connected to observe the results of the power-up tests.

1. Disconnect all inputs and exit all logic analysis sessions.

   In the Session Manager, select **Shutdown**. In the Powerdown window, select **Powerdown**.
2. When the "OK to power down" message appears, turn off the power switch.
3. After a few seconds, turn the power switch back on. Observe the boot dialogue for the following:
   - ensure all of the installed memory is recognized
   - any error messages
   - interrupt of the boot process with or without error message

   A complete transcript of the boot dialogue is in Chapter 8, "Theory of Operation".
4. During initialization, check for any failures.

See Also "The Power-Up Routine" in chapter 8.

To run the self-tests

Self-tests identify the correct operation of major functional subsystems of the instrument. You can run all self-tests without accessing the interior of the instrument. If a self-test fails, refer to the troubleshooting flowcharts to change a component of the instrument.

To run the self-tests:

1. In the System window, select System Admin.
2. In the System Administration window, select Self-Test. At the Test Query window, select Yes.

   The tests can be run individually, or all the tests can be run by selecting Test All at the bottom of the Self Test window. Note that if Test All is selected, tests requiring user action will not be run. For more information, refer to Chapter 8. These procedures instruct you how to perform the tests individually.
3. In the Self Test window, select System CPU Board.
4. Run the Flexible Disk Drive test.
   a. In the Self Test: System CPU Board window, select Floppy Drive Test.
   b. Insert a DOS-formatted flexible disk with 300 KB of available space in the flexible disk drive.
   c. In the Test Query window, select OK.

      The Test Query window instructs you to insert the flexible disk into the flexible disk drive. The other System CPU Board tests require similar user action to successfully run the test.
5. In the Self Test: System CPU Board window, select Close to close the window.
6. In the Self Test window, select PCI Board. The individual PCI Board tests can be run individually without any user action.
7. In the Self Test window, select the Master Frame tab. Individual tests can be run on the optional measurement module and emulation module in the Master Frame.

   Refer to Chapter 8 for more information on tests that are not executed. The service manuals for applicable measurement modules will also have information on tests that are not executed.

Reignite: Reinstalling the operating system

Read this section carefully before you attempt to reinstall the operating system using this procedure. Everything on the hard disk drive will be overwritten, including user configuration, data files, and license passwords.

A batch process is used to autoload the software and then reboot the instrument. The batch process waits for only a short timeout period for user interaction to abort the process. Otherwise, the hard disk drive will be initialized, the operating system uploaded, and the instrument will reboot.

The Reignite process takes approximately one hour depending on the speed of the CD-ROM.

See Also "To save the license file" in Chapter 6 for information on saving the license password file.

To reignite:

1. Set up the instrument.
   - **a** Connect the monitor, keyboard, and mouse to their rear panel ports.
   - **b** Connect a SCSI CD-ROM drive to the SCSI port on the rear of the instrument.
     Ensure the CD-ROM drive is set to a SCSI address in the range 1-5.
   - **c** Apply power to the CD-ROM drive.
   - **d** Insert the CD-ROM containing the instrument operating system into the CD-ROM drive.
     Allow a couple minutes for the CD-ROM drive to settle after inserting the media.
   - **e** If connected, disconnect the LAN cable from the instrument.
2. Connect the power cord to the instrument, and apply power to the instrument.
3. If needed, initiate the monitor selection mode.
   - **a** When the LED on the NUMLOCK key on the keyboard illuminates and remains lit approximately two seconds, press the [TAB] key. (This happens very soon after power is applied).
   - **b** When the monitor selection mode is enabled, repeatedly press the [TAB] key until the display is readable.
   - **c** Press the [ENTER] key, then answer "Y" at the query to confirm the monitor selection.
4. Interrupt the boot process and begin the Reignite process.
   - **a** Repeatedly press the [ESC] key on the keyboard to terminate the boot process.
   - **b** When the boot process is terminated, at the Main Menu: Enter command prompt, enter

     ```
     Main Menu: Enter command >  SEArch
     ```

     The instrument will then search for all viable boot devices on the bus. The display will then show the boot devices:

     ```
     Path Number      Device Path            Device Type
     -----------      -----------------      -----------
     P0               SESCSI.6.0             QUANTUM FIREBALL ST4.3S
     P1               SESCSI.4.0             IBM     CDRM00201     !F
     ```

   - **c** At the Main Menu: Enter command > prompt, enter

     ```
     Main Menu: Enter command > BOot P1
     Interact with IPL (Y, N, Q)?> N
     ```

   - **d** After about 30 seconds you will see the message

```
WARNING: The configuration information calls for a non-interactive
         installation.
         Press <Return> within 10 seconds to cancel
         batch-mode installation:
```

If you want to abort the Reignite process, go immediately to Step 5 below.

If you do nothing within the 10 second timeout, the Reignite process will begin. The instrument will completely reload the operating system software onto the hard disk drive. After the software has been uploaded, the instrument will reboot.

5 To abort the Reignite process at this point:

a Press [Return] within 10 seconds to abort the Reignite process.

b At the confirmation, press [Return] again.

c At the language prompt, enter 45. Press [RETURN] at the confirmation prompt.

d Enter b to reboot the system from the beginning.

To check the power supply voltages

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

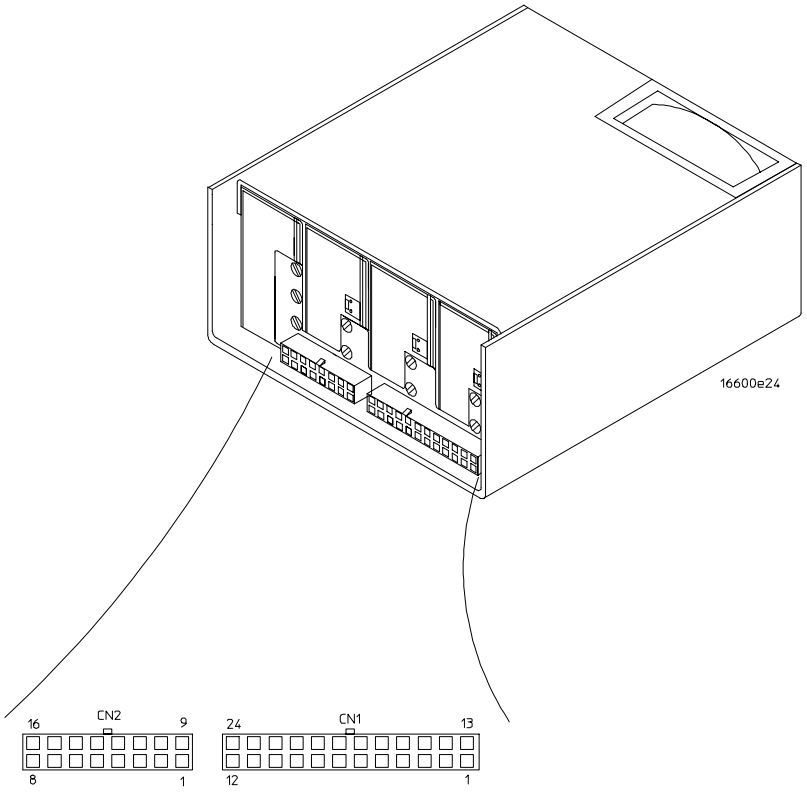
WARNING

Hazardous voltages exist on the power supply. This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.

1. Turn off the instrument, disconnect the power cord, then remove the cover.
2. Apply power to the instrument.
3. Using a DVM, measure the power supply voltages.
4. Note problems with the power supply, then return to the flowchart.

Power Supply Voltages

CN1		CN2	
Pin	**Voltage**	**Pin**	**Voltage**
1-5	+3.3 V	1-4	–5.2 V
6-7	COM	5	+12 V
8-10	+5 V	6-8	–12 V
11-12	COM	9-12	COM
13-14	+3.3 V	13	+12 V
15-19	COM	14-16	COM
20-21	+5 V		
22-24	COM		



To test the flexible disk drive voltages

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

WARNING

Hazardous voltages exist on the power supply. This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.

Equipment Required

Equipment	Critical Specification	Recommended Agilent Model/Part
Digitizing Oscilloscope	> 100 MHz Bandwidth	54600B

1. Turn off the instrument, then remove the power cable. Remove the cover of the logic analysis system.
2. Disconnect both the power cable and the data cable from the flexible drive.
3. Remove the two screws that secure the flexible drive to the frame and remove the flexible drive (refer to Chapter 6).
4. Reconnect the power and data cables to the flexible drive. Position the flexible drive so that it does not contact any of the other subassemblies or circuit boards inside the logic analysis system.
5. Reconnect the power cable to the instrument and apply power.
6. When the instrument completes the boot process, enter the Self Test menu and repetitively run the Floppy Drive Test.
   a. In the System menu, select System Admin.
   b. In the System Admin window, select Self Test. Select Yes at the confirmation dialogue box.
   c. When the Self Test window appears, select the System tab.
   d. In the Self Test window, select Options - Repeat Mode - Run Repeatedly.
   e. Insert a DOS-formatted flexible disk with at least 300 KB of available space into the flexible disk drive.
   f. Select System CPU Board. In the System CPU Board window, select Floppy Drive Test. At the Test Query window, select OK.

The floppy drive test will now run repetitively. Use an oscilloscope to probe the flexible disk drive signal pins (see table next page), to ensure that the digital signals are appearing.

Disk Drive Voltages

Pin	Signal Description	Pin	Signal Description	Pin	Signal Description
1	NC	13	Ground	24	Write Gate
2	Mode Select	14	NC	25	Ground
3	NC	15	Ground	26	Track 00
4	HD Out	16	Motor On	27	Ground
5	NC	17	Ground	28	Write Protect
6	NC	18	Direction	29	Ground
7	Ground	19	Ground	30	Read Data
8	Index	20	Step	31	Ground
9	Ground	21	Ground	32	Side One Select
10	NC	22	Write Data	33	Ground
11	Ground	23	Ground	34	Disk Change
12	Drive Select				

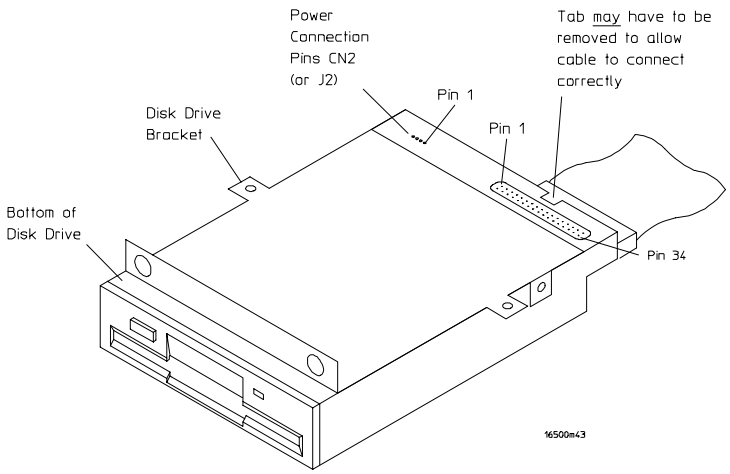
When you have completed probing the flexible disk drive signals, select OK in the Stop window do halt the Floppy Drive Test.

7 If the flexible disk drive signals appear as indicated, then the flexible disk drive should be replaced. If the signals do not appear, then either the data cable or the CPU board is suspect.

J11 of the acquisition board can be probed in the same manner as described above to check for the same signals.

8 Remove power from the logic analysis system and disconnect the power cable. Replace the defective assembly.

9 Reassemble the logic analysis system.



To test the hard disk drive voltages

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

WARNING

Hazardous voltages exist on the power supply. This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.

Equipment Required

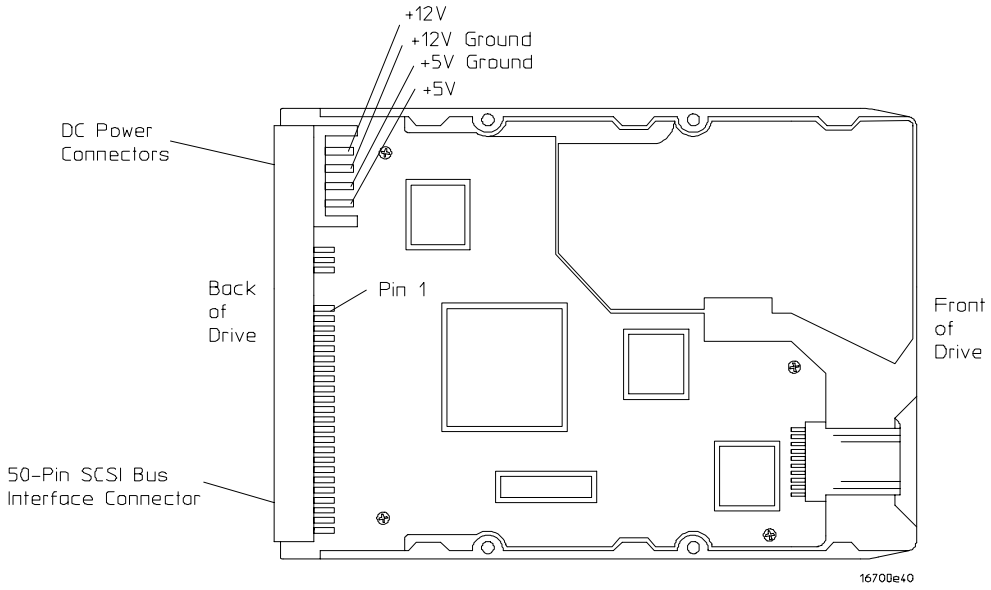
Equipment	Critical Specification	Recommended Model/Part
Digitizing Oscilloscope	> 100 MHz Bandwidth	54600B

1. Turn off the instrument, then remove the power cable. Remove the cover of the logic analysis system.
2. Disconnect both the power cable and the data cable from the hard drive.
3. Remove the two screws that secure the hard drive to the frame and remove the hard drive (refer to Chapter 6).
4. Remove four screws that secure the mounting plate to the hard drive and remove the mounting plate.
5. Reconnect the power and data cables to the hard drive. Position the hard drive so that it does not contact any of the other subassemblies or circuit boards inside the logic analysis system.
6. Reconnect the power cable to the instrument and apply power.
7. Using an oscilloscope, check for digital activity on the pins while the instrument is booting. Probe the voltages on the hard disk drive circuit board where the data cable connector is soldered. Pin 1 of the connector is marked on the circuit board and is on the side of the connector closest to the power cable (see table and illustration next page).

Disk Drive Voltages

Pin	Signal Description	Pin	Signal Description
2	DB0	28	NC
4	DB1	30	Ground
6	DB2	32	ATN
8	DB3	34	Ground
10	DB4	36	BSY
12	DB5	38	ACK
14	DB6	40	RST
16	DB7	42	MSG
18	DBP	44	SEL
20	Ground	46	C/D
22	Ground	48	REQ
24	NC	50	I/O
26	Terminator Power		

All odd-numbered pins except 23, 25, and 27 are grounded at the drive. Pins 24 and 28 are "No Connect" at the drive.



8 If the hard disk drive signals appear as indicated, then the hard disk drive should be replaced. If the signals do not appear, then either the data cable or the CPU board is suspect.

   J1 and J10 of the PCI board can be probed in the same manner as described above to check for the same signals.

9 Remove power from the logic analysis system and disconnect the power cable. Replace the defective assembly.

10 Reassemble the logic analysis system.

To test the cables

This test allows you to functionally verify the probe cable and probe tip assembly of any of the logic analyzer pods. Only one probe cable can be tested at a time. Repeat this test for each probe cable to be tested.

Equipment Required

Equipment	Critical Specification	Recommended Agilent Model/Part
Pulse Generator	100 MHz, 3.5 ns pulse width, < 600 ps rise time	8131A Option 020
6x2 Test Connectors (Qty 4)		

1 If you have not already done so, do the procedure "To set up the test equipment and the logic analyzer" in Chapter 3.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Trigger
Mode: Ext Period: 100.000 ns	Mode: Square Delay: 0.000 ns High: 3.00 V Low: 0.00 V COMP: Disabled (LED Off)	Divide: Divide ÷ 1 Ampl: 0.50 V Offs: 0.00 V

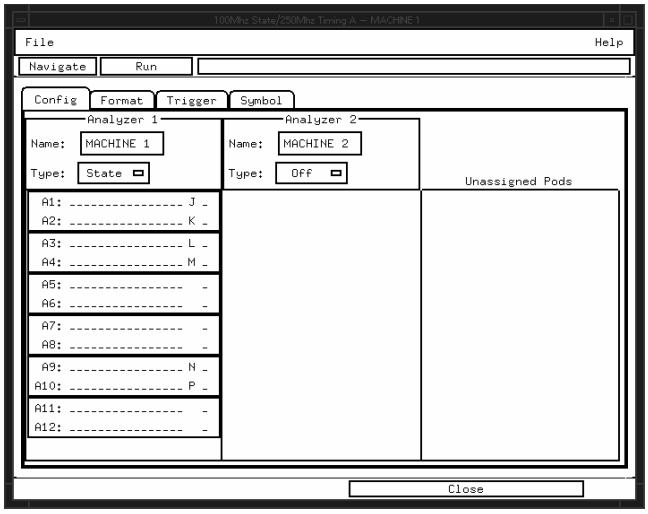
b Enable the pulse generator channel 1 and channel 2 outputs (LED off).

3 Set up the Configuration window.

a In the MACHINE 1 window, select the Config tab.

b Ensure that they Type analyzer is set to State.

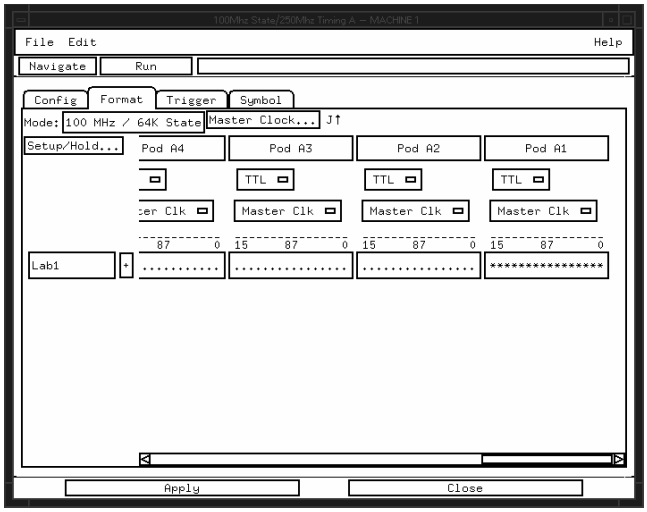
c Assign all pods to Analyzer 1. To assign the pods, use the mouse to drag the pods to the Analyzer 1 column (see figure on next page).



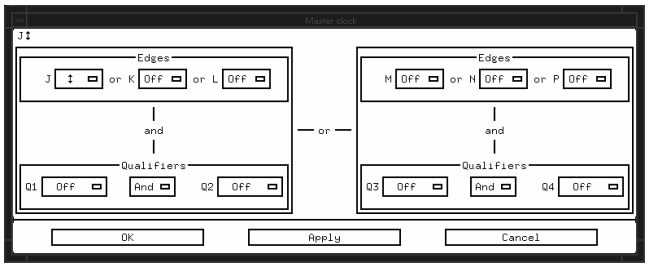
4 Set up the Format window.

a In the MACHINE 1 setup window, select the Format tab.

b Select the field showing the channel assignments for the pod under test. In the pop-up menu, select the asterisk field to put asterisks in the channel positions, activating the channels. Select Done.



c Select Master Clock. In the Master Clock window, select a double edge for the J clock (J↕). Turn off the other clocks. Select Apply, then select OK to close the Master Clock window.



d Select Setup/Hold, then select 5.0/0.0 ns for the pod being tested. Select OK to close the Setup/Hold window.

e Select the threshold field for the pod being tested, then select TTL.

6 Set up the Trigger window.

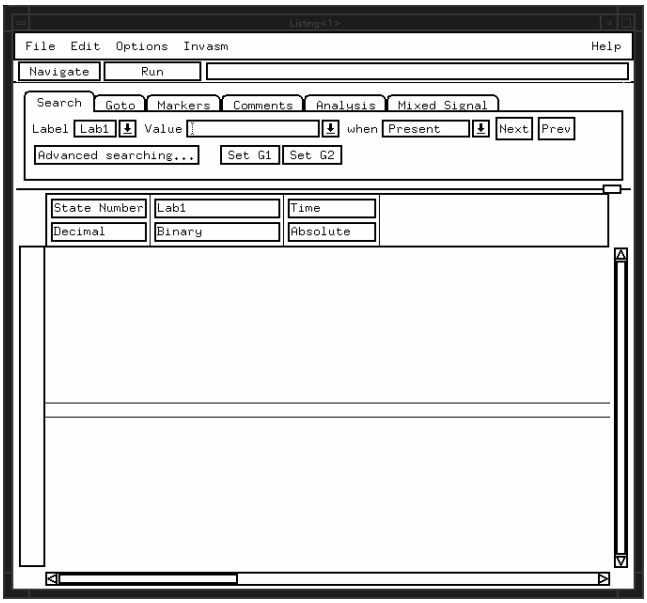
a In the MACHINE 1 setup window, select the Trigger tab.

b Select Clear, then select All.

7 Set up the Listing window.

a In the MACHINE 1 Setup window, select Navigate, then select Slot A: MACHINE 1, then select Listing. A Listing window will open.

b Right click on the hex field and change the Lab1 base to Binary.



8 Using four 6-by-2 test connectors, connect the logic analyzer to the pulse generator channel outputs. To make the test connectors, see chapter 3, "Testing Performance."

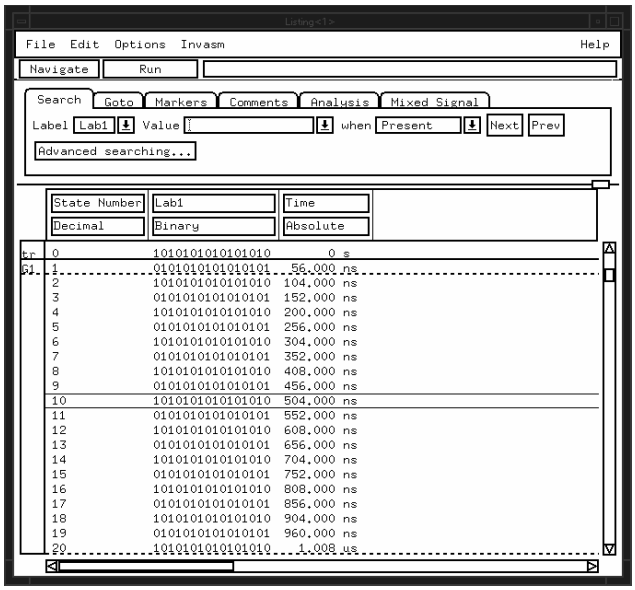
a Connect the even-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 Output.

b Connect the odd-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 $\overline{\text{Output}}$.

c Connect the even-numbered channels of the upper byte of the pod under test and the J clock channel to the pulse generator channel 2 Output. J clock is located on Pod A1.

d Connect the odd-numbered channels of the upper byte of the pod under test to the pulse generator channel 2 $\overline{\text{Output}}$.

9 On the logic analyzer, select Run. The listing should look similar to the figure below. Ignore any error messages dealing with the G1 and G2 markers.



10 If the listing looks like the figure, then the cable passed the test.

If the listing does not look similar to the figure, then there is a possible problem with the cable or probe tip assembly. Causes for cable test failures include:

- open channel.
- channel shorted to a neighboring channel.
- channel shorted to either ground or a supply voltage.

Return to the troubleshooting flowchart.

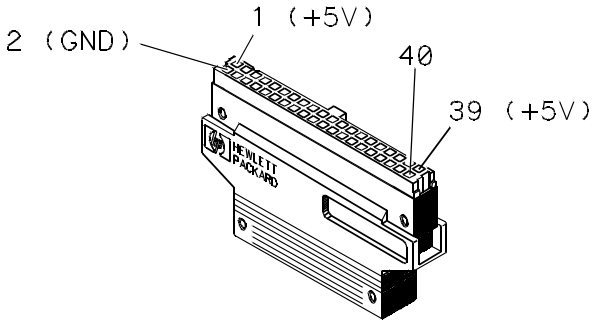
To test the auxiliary power

The +5 V auxiliary power is protected by a current overload protection circuit. If the current on pins 1 and 39 exceed 0.33 amps, the circuit will open. When the short is removed, the circuit will reset in approximately 1 minute. There should be +5 V after the 1 minute reset time.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	na	E2373A

- Using the multimeter, verify the +5 V on pins 1 and 39 of the probe cables.



MISC/EX50

To troubleshoot initialization failures

By the time the logic analysis system reaches the initialization phase during the boot process, the core subsystems have been tested and are operating. During initialization, the system is being configured to run the operating system software.

A FAIL status during initialization does not necessarily mean there is a serious problem or catastrophic failure of the hardware. Failures are often generated because of changes in the configuration of the hardware or of the system. Occasionally a FAIL status is caused by software file corruption.

If the logic analysis system is part of an equipment pool that is shared among a number of users, then some of the network-related initializations can result in a FAIL as some users utilize the networking capabilities of the instrument.

If a FAIL status is reported during initialization, then most likely the system is still usable if initialization completes, the entire boot process completes, and the System window appears. If the boot process halts (with or without an error message), then a system problem must be corrected before the logic analysis system is usable.

On the logic analysis system display, the initialization phase of the boot process looks like this:

```
HP-UX Start-up in progress                        Status
_________________________                         ______
Mount file systems ............................. [ OK ]
Setting hostname ............................... [ OK ]
Enable auxiliary swap space .................... [ OK ]
Start syncer daemon ............................ [ OK ]
Configure LAN interfaces ....................... [ OK ]
Start Software Distributor agent daemon ........ [ OK ]
Clean up old log files ......................... [ OK ]
Start system message logging daemon ............ [ OK ]
Configure HP Ethernet interfaces ............... [ OK ]
Configure LAN interfaces ....................... [ OK ]
Start NFS core subsystem ....................... [ OK ]
Start NFS client subsystem ..................... [ OK ]
Start Internet services daemon ................. [ OK ]
Start time synchronization ..................... [N/A ]
Start print spooler ............................ [ OK ]
Start clock daemon ............................. [ OK ]
Set X11 Device Configuration ................... [ OK ]
Start HP16700 Processor Run Control daemon .... [ OK ]
Start NFS server subsystem ..................... [ OK ]
Start Lngrd daemon ............................. [ OK ]
```

Mount file systems: most likely cause is a hard disk drive hardware failure that was not found earlier in the boot process. A secondary cause of a FAIL status is the cables of the hard disk drive are not properly seated in the disk drive or in the PCI board.

Setting hostname: the most likely cause is a change of network configuration.

Enable auxiliary swap space: unlikely failure.

Start syncer daemon: unlikely failure.

Configure LAN interfaces: the most likely cause is a hardware failure of the CPU board that was not found earlier in the boot process, or a hardware failure of the PCI board. If a LAN cable is not connected to the 10BaseT port, or if a 50 ohm termination is not connected to the 10Base2 port, a FAIL may also be reported.

Start Software Distributor agent daemon: the most likely cause is a networking or port configuration. A secondary cause of a FAIL status is corrupted software.

Clean up old log files: unlikely failure.

Start system message logging daemon: unlikely failure.

Configure HP Ethernet interfaces: the most likely cause is networking configuration.

Configure LAN interfaces: more LAN configuration is performed here. The failure modes are the same as above.

Start NFS core subsystem: unlikely failure.

Start NFS client subsystem: a FAIL status is returned when the instrument is connected to a LAN, the networking configuration is not correct (especially the IP address and subnet mask), and/or a remote workstation that was mounted to the instrument file system configured as Mount Always is no longer available. The quickest workaround of a FAIL status is to disconnect the LAN cable if the instrument will not be networked.

Start Internet services daemon: the most likely cause is networking configuration.

Start time synchronization: always returns N/A because this feature is disabled.

Start print spooler: the most likely cause of failure is a hardware failure of the CPU parallel port. A N/A status is caused when the print spooler is disabled.

Start clock daemon: unlikely failure.

Set X11 Device Configuration: unlikely failure.

Start HP16700 Processor Run Control daemon: the most likely cause of failure is a corrupted configuration file for the emulation module. A secondary cause of a FAIL status is a hardware failure of the PCI board or of the emulation module itself, if installed.

Start NFS server subsystem: the most likely cause is networking configuration.

Start Lngrd daemon: the most likely cause is networking configuration.

6

Replacing Assemblies

Replacing Assemblies

This chapter contains the instructions for removing and replacing the assemblies of the logic analysis system. Also in this chapter are instructions for returning assemblies.

WARNING

Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least six minutes for the capacitors on the power supply board to discharge before servicing the instrument.

CAUTION

Damage can occur to electronic components if you remove or replace assemblies when the instrument is on or when the power cable is connected. Never attempt to remove or install any assembly with the instrument on or with the power cable connected.

Replacement Strategy

These replacement procedures are organized as if disassembling the complete instrument, from the first assembly to be removed to the last. Some procedures say to remove other assemblies of the instrument, but do not give complete instructions. Refer to the procedure for that specific assembly for the instructions.

CAUTION

Electrostatic discharge can damage electronic components. Use grounded wrist straps and mats when performing any service to this logic analyzer.

Tools Required

T8, T10, T15, T25 TORX screwdrivers
#1 Posidrive screwdriver
1/8-inch screwdriver
13/16-inch deep-well nutdriver
3/16-inch nutdriver
3/8-inch deep-well nutdriver

To save the license file

Before doing any major repairs to the instrument, it is recommended that you back up the license file if possible. You will need a back up copy if you encounter any problems that require a software Reignite.

The license file has all of the licenses for the toolsets and user registration. If for some reason you lose the license file, you can obtain new license codewords from the Agilent password center.

To save the license file:

1. Obtain a formatted flexible disk and insert it in the flexible disk drive.
2. In the System window, select File Manager.
3. In the `/hplogic/licensing` subdirectory, copy the `license.dat` file to the flexible disk.

To recover passwords

The password file `/hplogic/licensing/license.dat` may be lost under any of the following circumstances:

- Catastrophic failure of the hard disk drive
- Software Reignite
- User error
- Instrument sent to an Agilent Technologies Service Center with Secure mode enabled

To avoid losing the license.dat file, back up the file onto a flexible disk and keep the disk in a safe place. The `license.dat` file can also be archived in any DOS or HP-UX environment.

If the license.dat file (which includes the passwords) is lost, any activated toolsets will become unavailable and the User Registration window will again become visible. To recover the passwords and re-create a license.dat file, you must contact the Agilent Password Center. Provide the instrument ID number to the Password Center, and they will re-issue your passwords. Refer to your on-line help menu for information on contacting your local Agilent Password Center.

An Agilent Technologies Service Center can contact the Agilent Password Center after an instrument repair to recover toolset passwords. The Agilent Technologies Service Center must provide the instrument ID number to the Agilent Password Center to recover the toolset passwords. However, you must contact the Agilent Password Center to recover your User Registration password.

To obtain the instrument ID

The instrument ID can be found in the System Administration window under the **Admin - [About]** button.

The procedures in the following sections cover assembly and disassembly of the 16600A-series Logic Analysis System.

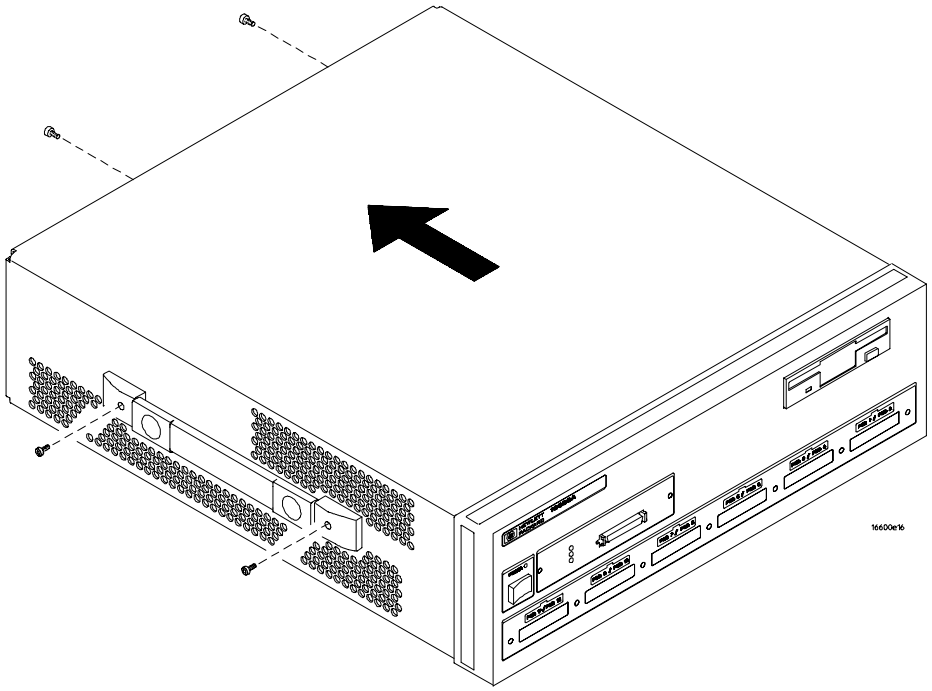
To remove and replace optional measurement module or filler panel

1. Remove power from the instrument.
   - **a** Exit all logic analysis sessions. In the session manager ,select Shutdown.
   - **b** At the query, select Power Down.
   - **c** When the "OK to power down" message appears, turn the instrument off.
   - **d** Disconnect the power cord.
2. Loosen the thumbscrews on the module or filler panel and remove the module or filler panel from the mainframe.
3. Reverse this procedure to install the module or filler panel.

   When installing a module, ensure the module is properly seated in the module interface board. Apply pressure to the center of the module rear panel while tightening the thumbscrews.

To remove and replace the cover

1. Remove power from the instrument.
   a. Exit all logic analysis sessions. In the session manager ,select Shutdown.
   b. At the query, select Power Down.
   c. When the "OK to power down" message appears, turn the instrument off.
2. Disconnect the power cable and all data and peripheral cables from the rear panel.
3. Move the instrument to a static-safe work area before beginning any disassembly.
4. Using a Torx T15 screwdriver, remove the two screws in the endcaps of the handle, then lift off the handle.
5. Using a Torx T10 screwdriver, remove two screws that secure the cover to the rear panel.



6. Slide the cover toward the rear of the instrument until it is all of the way off.
7. Reverse this procedure to install the cover.

   Check that all assemblies are properly installed before installing the cover.

   When installing the cover, ensure that the tabs located at the bottom rear of the cover align with the holes on the rear panel.

To remove and replace the hard disk drive

1 Using previous procedures, remove the following assemblies:

- Cover

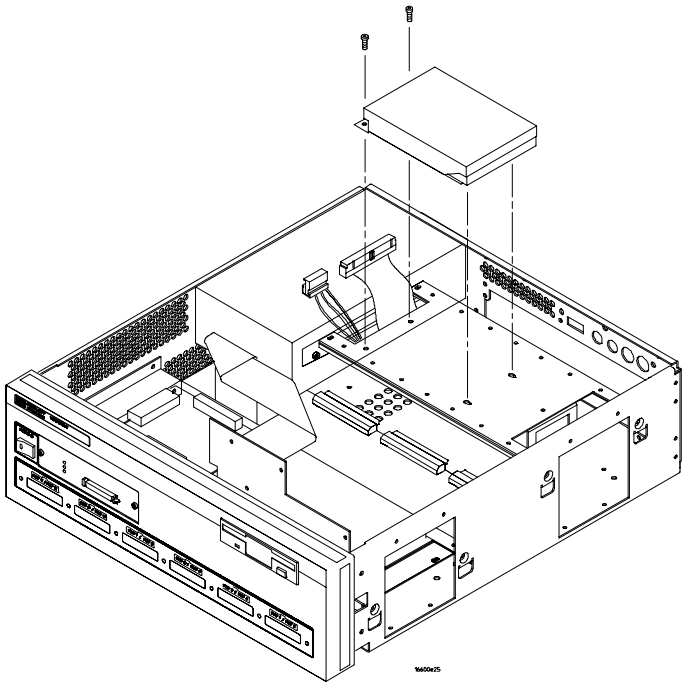
2 Disconnect the hard disk drive power cable and data cable from the rear of the hard disk drive.

If the hard disk drive is being removed only to gain access to another subassembly in the instrument, skip steps 3-6 and proceed directly to step 7. The hard disk drive and the rear plate will therefore be removed as one unit.

3 Using a Torx T10 screwdriver, remove two screws that secure the hard disk drive bracket to the rear plate.

4 Slide the hard disk drive toward the power supply approximately 0.5 cm.

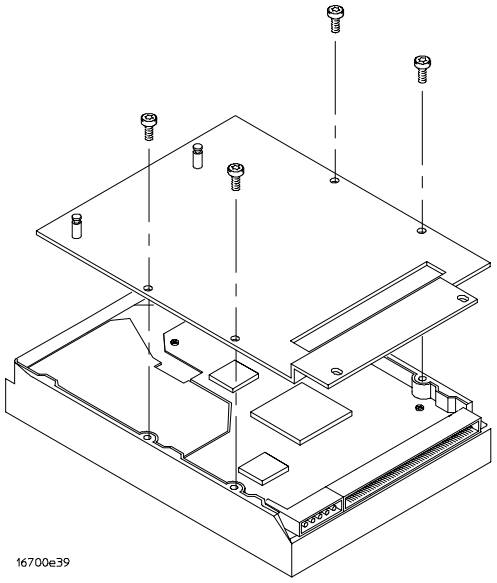
5 Lift the hard disk drive out of the instrument.



6 If needed, remove the hard disk drive bracket from the hard disk drive.

a Using a Torx T15 screwdriver, remove four screws that secure the hard disk drive bracket to the hard disk drive.

b Remove the bracket from the hard disk drive.



7 If needed, remove the rear plate.

a If installed, remove the measurement module from the instrument.

b Using a Torx T10 screwdriver, remove two screws that secure the rear plate to the power supply.

c Using a Torx T10 screwdriver, remove two screws that secure the rear plate to the side panel of the deck.

d Lift the rear plate out of the instrument.

8 Reverse this procedure to install the hard disk drive.

Before installing the hard disk drive, ensure the following assemblies are properly installed:

- Power Supply
- PCI Board
- CPU board
- Acquisition Board

When installing the hard disk drive/bracket assembly onto the rear plate, ensure the metal standoffs on the disk drive bracket are properly seated in the corresponding holes in the tray.

After replacing the hard disk drive and reassembling the instrument, follow the procedure "Catastrophic Failure Recovery" in this chapter to reload the hard disk drive.

To remove and replace the flexible disk drive

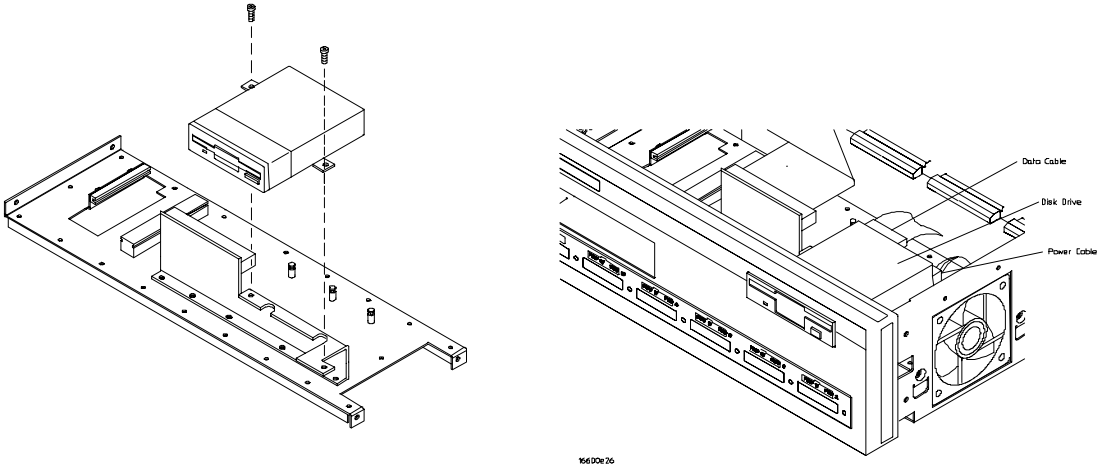
1 Using previous procedures, remove the following assemblies:

- Cover

2 Disconnect the flexible disk drive power cable and data cable from the rear of the flexible disk drive.

The flexible disk drive power cable connector has a tab. Lift up slightly on the rear of the connector while disconnecting the cable from the flexible disk drive.

3 Using a Torx T10 screwdriver, remove the two screws that secure the flexible disk drive plate to the flexible disk drive bracket.



4 Slide the flexible disk drive toward the rear of the instrument approximately 0.5 cm.

5 Tilt up the rear of the flexible disk drive, then lift the flexible disk drive out of the instrument.

6 If needed, remove the flexible disk drive plate from the flexible disk drive.

a Using a Torx T10 screwdriver, remove the four screws that secure the flexible disk drive plate to the flexible disk drive.

b Remove the plate from the flexible disk drive.

7 Reverse this procedure to install the flexible disk drive.

Before installing the flexible disk drive, ensure the following assemblies are properly installed:

- Acquisition Board

To remove and replace the optional emulation module

1 Using previous procedures, remove the following assemblies:

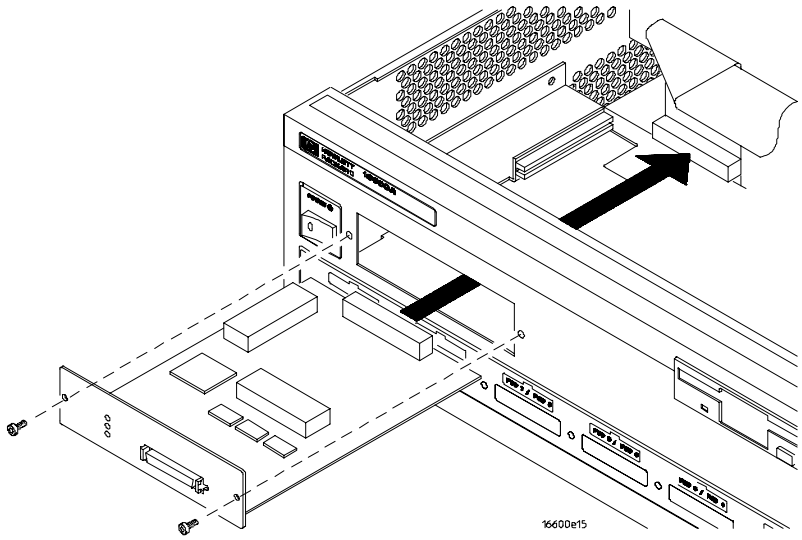
- Cover

2 Disconnect the module interface cable from the emulation module

The module interface cable has tabs on the ends of the connector. Squeeze the connector tabs with thumb and forefinger while disconnecting the cable.

3 Using a Torx T10 screwdriver, remove the two screws on the front panel that secure the emulation module to the front panel.

4 Slide the emulation module out the front of the instrument.



5 Reverse this procedure to install the emulation module.

To remove and replace the module interface board

1 Using previous procedures, remove the following assemblies:

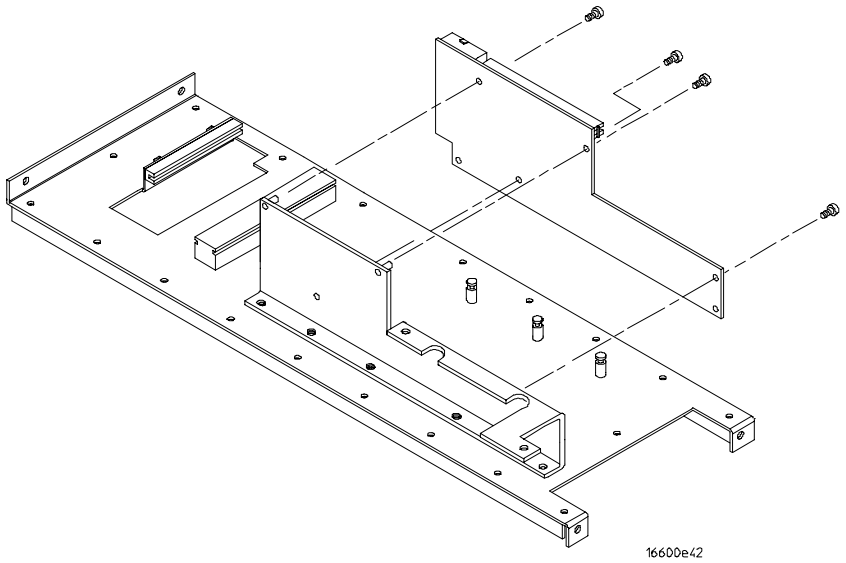
- Measurement Module (if installed)
- Cover
- Flexible Disk Drive

2 Disconnect the power cable and module interface cable from the module interface board.

The power cable has a lock at the top of the connector. Press the tab at the rear of the connector to release the lock while disconnecting the cable. The module interface cable has tabs on the ends of the connector. Squeeze the connector tabs with thumb and forefinger while disconnecting the cable.

3 Using a Torx T10 screwdriver, remove the four screws that secure the module interface board to the disk drive bracket.

4 Lift the module interface board out of the instrument.



5 If needed, remove the front plate from the deck.

a If installed, remove the emulation module using previous procedures.

b If present, remove the CPU board.

c Using a Torx T10 screwdriver, remove the four screws, two from each side of the deck, that secure the front plate to the deck.

d Lift the front plate out of the instrument.

6 Reverse this procedure to install the module interface board.

Before installing the module interface board, ensure the following assemblies are properly installed:

- Acquisition Board

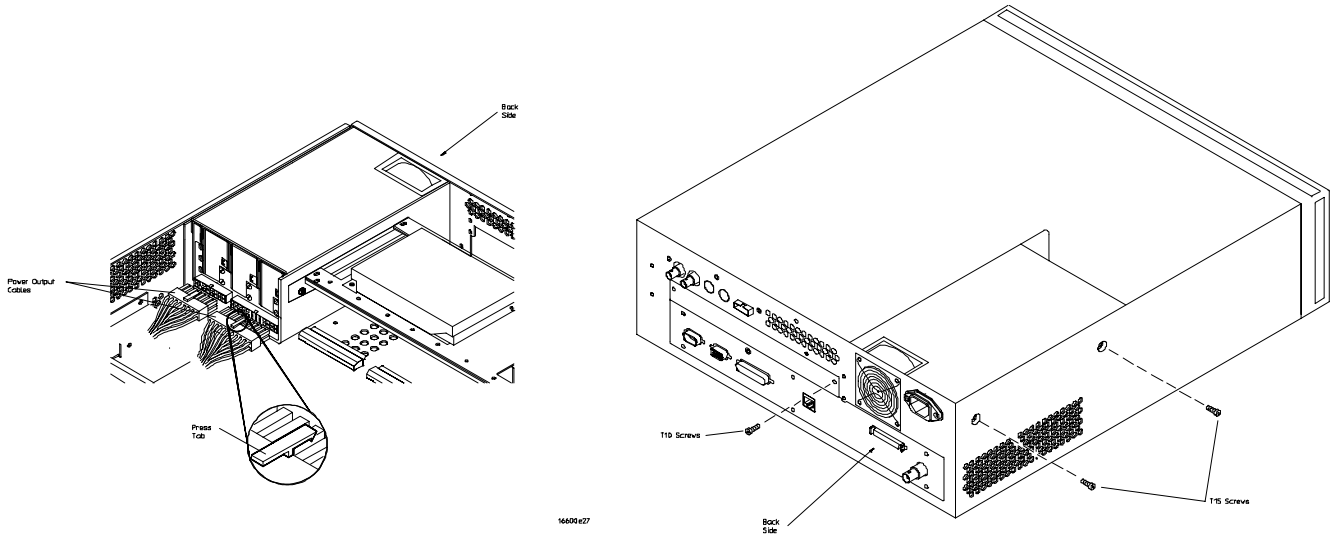
To remove and replace the power supply

WARNING

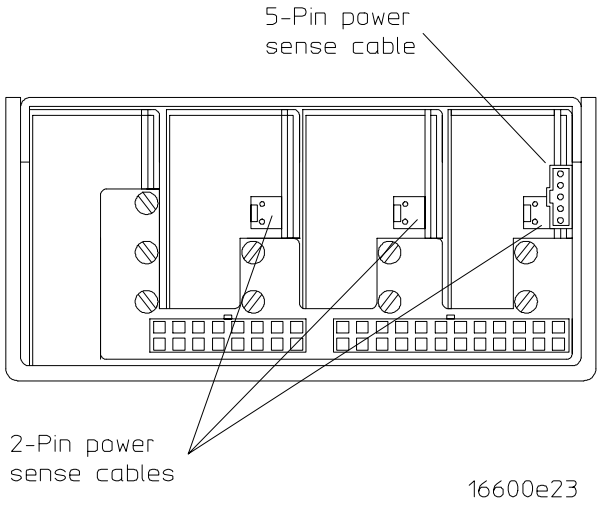
Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect the power from the instrument before performing the following procedure. After disconnecting the power, wait at least six minutes for the capacitors on the power supply board to discharge before servicing the instrument.

1. Using previous procedures, remove the following assemblies:
   - Cover
   - Hard Disk Drive (with rear plate)
2. Disconnect the power output cables (large gauge white) from the output connectors on the power supply.
3. Disconnect the power sense cable from the acquisition board (J18).

   The power cables have a lock at the top of each connector. Press the tab at the rear of the connector to release the lock while disconnecting each cable.
4. Using a #1 Posidrive screwdriver, remove the power input cable from the power supply input terminal block.
5. Using a Torx T10 screwdriver, remove one screw that secures the power supply to the rear of the deck.
6. Using a Torx T15 screwdriver and while holding the power supply, remove two screws that secure the power supply to the side of the deck.
7. Remove the power supply out of the instrument.



8 If needed, remove the power sense cable from the power supply. Mark the three 2-pin power sense cables so that you can re-connect them to the same connectors when installing the power supply.



9 If needed, remove the power supply bracket from the power supply.

a Using a Torx T15 screwdriver, remove two screws that secure the power supply bracket to the power supply.

b Remove the bracket from the power supply.

10 Reverse this procedure to install the power supply.

Before installing the power supply, ensure the following assemblies are properly installed:

- PCI Board
- CPU Board
- Acquisition Board

To remove and replace the PCI board

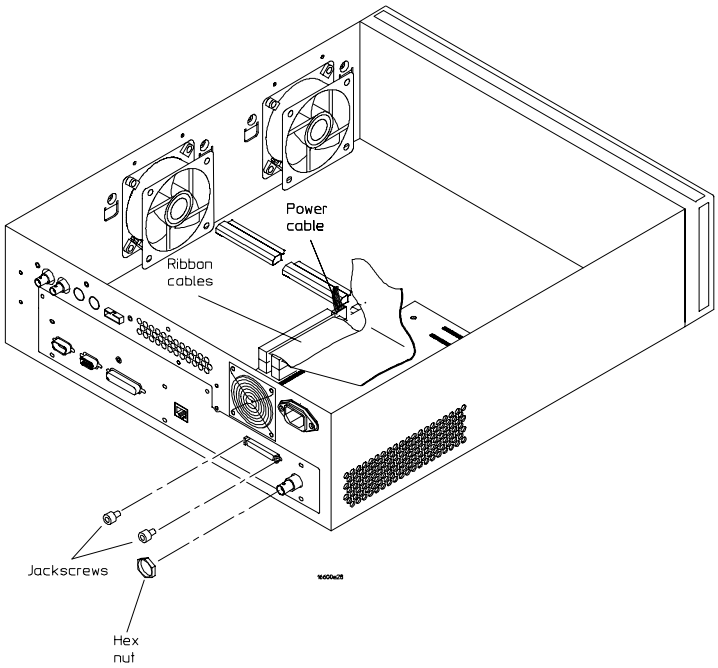
1 Using previous procedures, remove the following assemblies:
- Cover
- Hard Disk Drive (with rear plate)
- Power Supply

2 Disconnect the I/O cable from the PCI board.

The I/O cable has tabs on the ends of the connector. Squeeze the connector tabs with thumb and forefinger while disconnecting the cable.

3 Using a 1/8-inch flat blade screwdriver, remove the jackscrews that secures the SCSI connector to the rear panel.

4 Using a deep well 13/16-inch nutdriver, remove the hex nut that secures the LAN BNC to the rear panel.

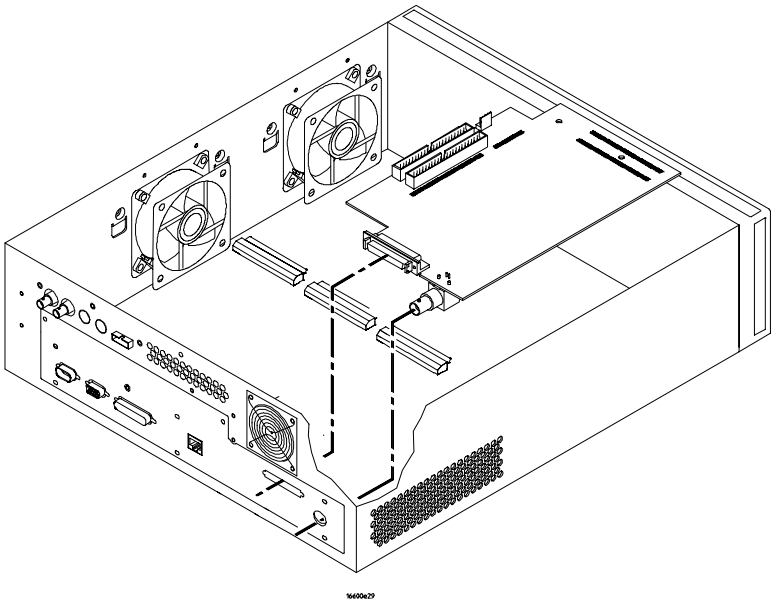


5 Using a #1 Posidrive screwdriver, remove two screws that secure the PCI board to the standoffs on the CPU board.

6 While using your thumb to release the locking tab on the side of the board, gently lift up the edge of the board that is toward the front of the instrument.

The PCI board does not slide right out of the instrument. There are three connectors on the bottom of the board that interface the PCI board to both the CPU board and the acquisition board.

7 After the interface connectors have disengaged from the CPU board and acquisition board, lift the PCI board out the instrument.



8 Reverse this procedure to install the PCI board.

When installing the PCI board, first align the guide hole on the board to the guide post that is next to the locking tab. Align the three interface connectors on the bottom of the PCI board to the corresponding connectors on the CPU board and acquisition board. A slight pressure of the board against the rear panel may be necessary to begin the alignment of the connectors.

Before installing the hard disk drive, ensure the following assemblies are properly installed:

- CPU Board
- Acquisition Board

To remove and replace the CPU board

1 Using previous procedures, remove the following assemblies:

Measurement Module (if installed)

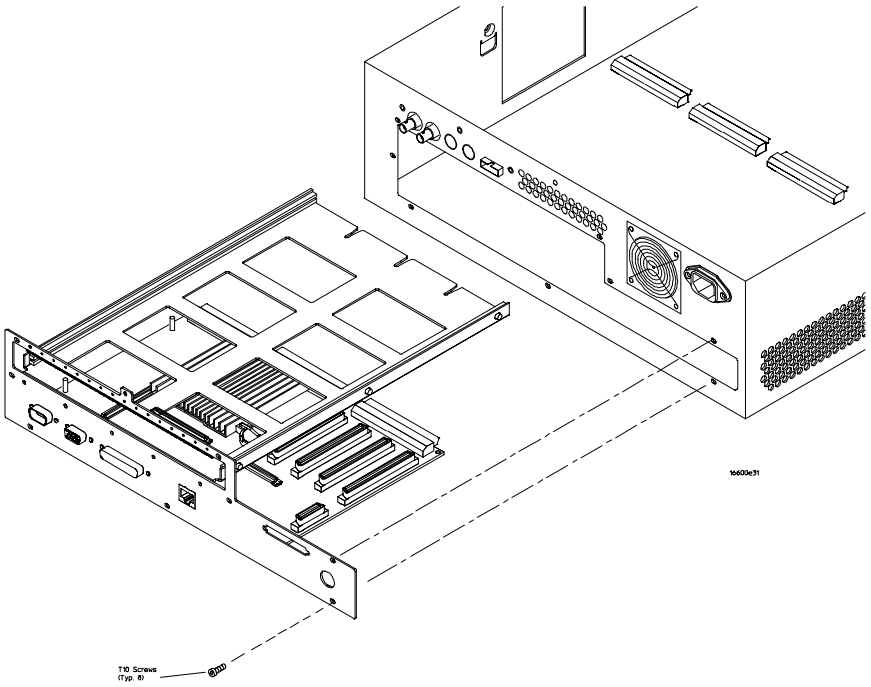
- Cover
- Hard Disk Drive (with rear plate)
- Power Supply
- PCI Board

2 Using a Torx T10 screwdriver, remove six screws that secure the CPU back panel to the rear panel of the instrument.

3 Slide the CPU board out the rear of the instrument. As you remove the CPU board, it will become disconnected from the acquisition board.

CAUTION Do not use component heat sinks as leverage in removing the CPU board. Damage to the CPU board components will result.

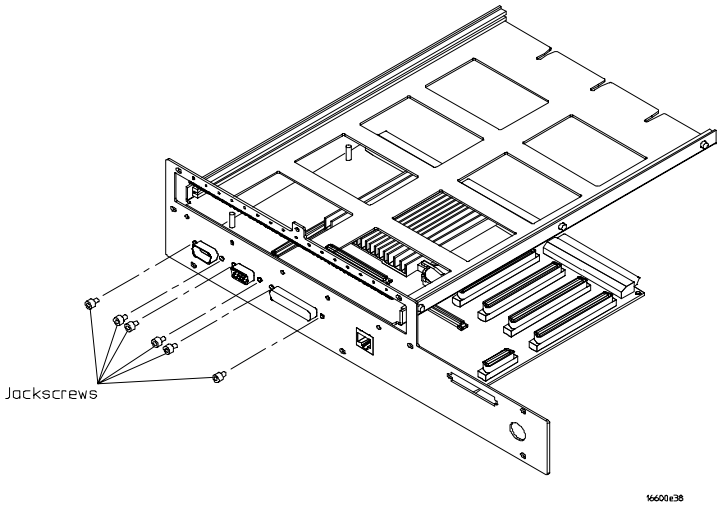
CAUTION Do not pry the CPU board from the interface board by inserting a flat blade screwdriver and twisting the screwdriver. Damage to the circuit board will result.



4 Remove the CPU back panel from the CPU board.

a Using a 3/16-inch nutdriver, remove the jackscrews that secure the RS-232-C, video, and parallel printer connectors from the CPU rear panel.

b Remove the rear panel from the CPU board.



5 Exchange System RAM and Video RAM (if installed) between the defective and replacement CPU boards.

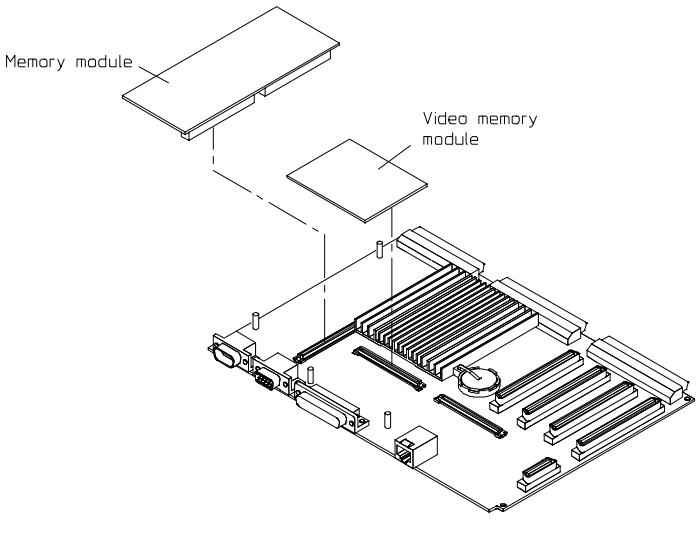
a Remove the System RAM daughter card by lifting the daughter card off the CPU board.

b If installed, remove the Video RAM card by lifting the card off the CPU board.

c Position the daughter card from the defective CPU board over the replacement CPU board. Align both the connectors and the standoffs on the CPU board with the connectors and holes on the daughter card.

d Repeat step c for the Video RAM, if installed.

e Repeat steps c and d to install the daughter card and the Video RAM card from the replacement CPU board onto the defective CPU board.



5 Reverse this procedure to install the CPU board.

Before installing the CPU board, ensure the following assemblies are properly installed:

- Acquisition Board

After replacing the CPU board and reassembling the instrument, follow the procedure "Catastrophic Failure Recovery" in this chapter to reconfigure the CPU board.

To remove and replace the acquisition board

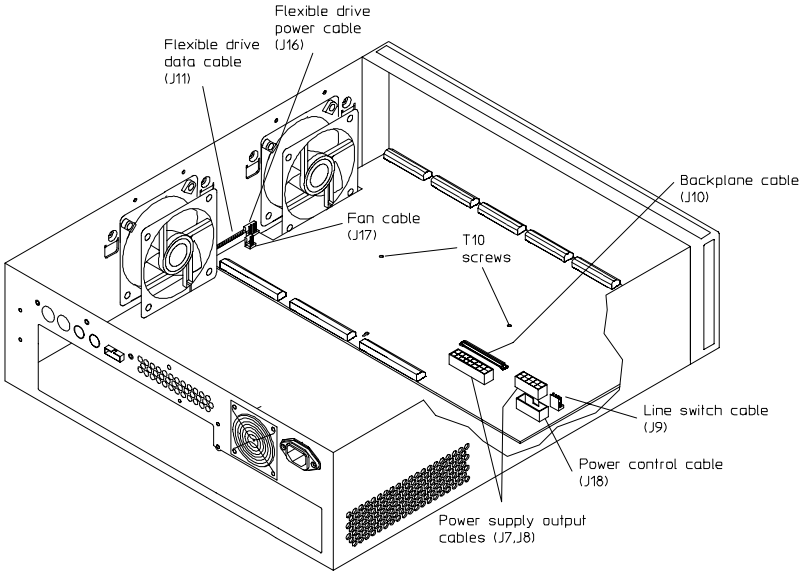
1 Using previous procedures, remove the following assemblies:
- Measurement Module (if installed)
- Cover
- Hard Disk Drive (with rear plate)
- Flexible Disk Drive
- Run Control Board (if installed)
- Power Supply
- PCI Board
- CPU Board
- Module Interface Board (with front plate)

2 Using a Torx T10 screwdriver, remove the screws that secure the probe cables to the front panel of the instrument.

3 Disconnect the following cables:
- Flexible Disk Drive data cable (J11)
- Flexible Disk Drive power cable (J16)
- Fan cable (J17)
- Line switch cable (J9)
- Backplane Cable (J10)
- Power supply power output cable (J7 and J8)

4 Using a Torx T10 screwdriver, remove two screws at the center of the acquisition board that secures the board to the deck.

5 Slide the acquisition board toward the rear of the instrument approximately 0.5 cm.



6 Lift the acquisition board out of the instrument.

7 Reverse this procedure to install the acquisition board.

Before installing the acquisition board, ensure the ground strips are installed one per pod cable connector on the front of the acquisition board.

To remove and replace the fan

1 Using previous procedures, remove the following assemblies:

- Measurement Module (if installed)
- Cover
- Hard Disk Drive (with rear plate) *
- CPU Board *
- Module Interface Board (with front plate) *

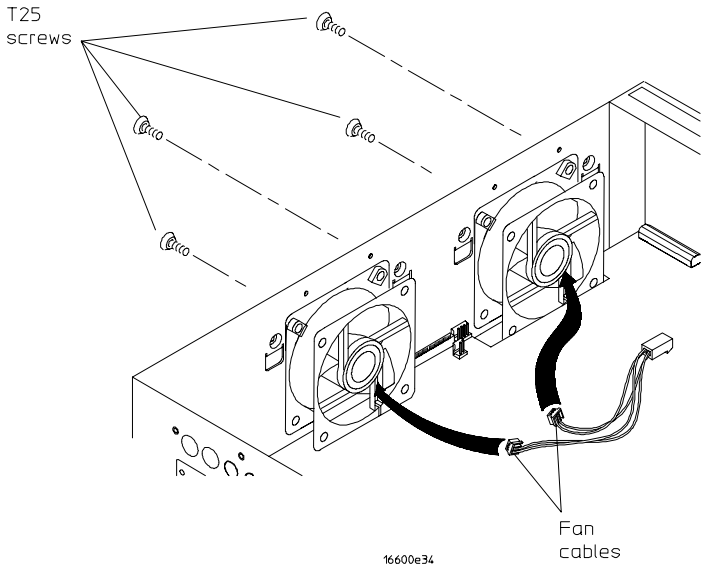
  * depending on which fan will be replaced

2 Disconnect the fan cable from the fan to be replaced. After the connector becomes disengaged from the connector pins on the fan, pull the connector out and away from the fan.

3 Using a #1 Posidrive screwdriver, remove four screws, one at each corner of the fan, that secures the fan to the side of the deck.

4 Using a 1/8-inch flat blade screwdriver, push out the screw inserts enough to be able to grab them with a thumb and forefinger.

5 While holding the fan, remove the four screw inserts, one at each corner of the fan.



6 Reverse this procedure to install the fan.

When installing the fan, ensure the cable notch on the fan assembly is pointing toward the flexible disk drive data cable.

To remove and replace the I/O board

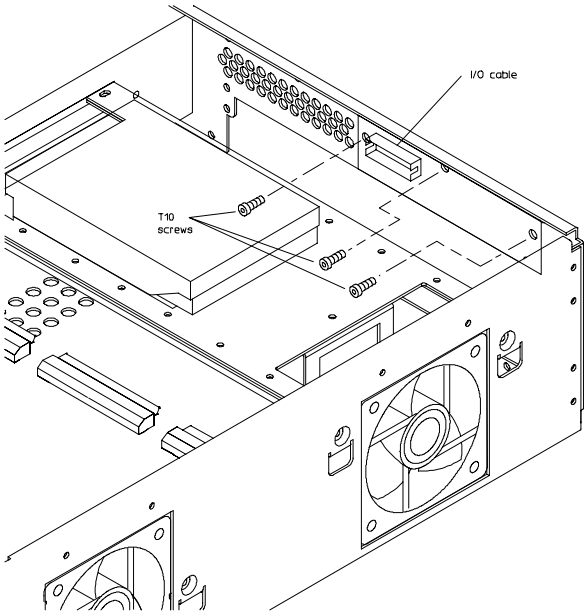
1 Using previous procedures, remove the following assemblies:

- Cover

2 Disconnect the I/O cable from the I/O board.

The I/O cable has tabs on the ends of the connector. Squeeze the connector tabs with thumb and forefinger while disconnecting the cable.

3 Using a Torx T10 screwdriver, remove three screws that secure the I/O board to the rear panel.



4 Reverse this procedure to install the I/O board.

To remove and replace the front panel and front frame

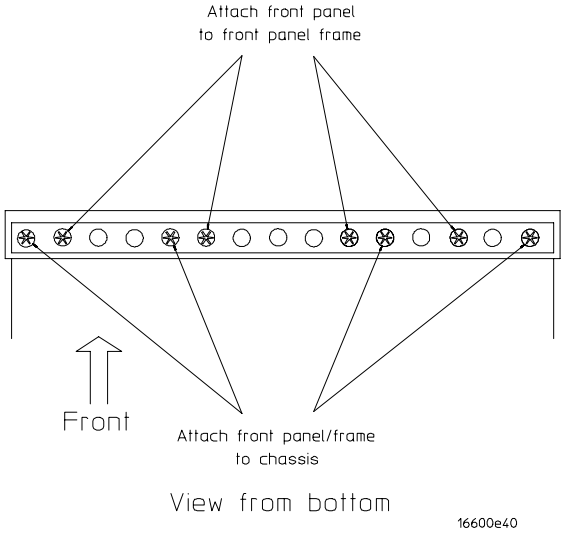
1 Using previous procedures, remove the following assemblies:

- Cover

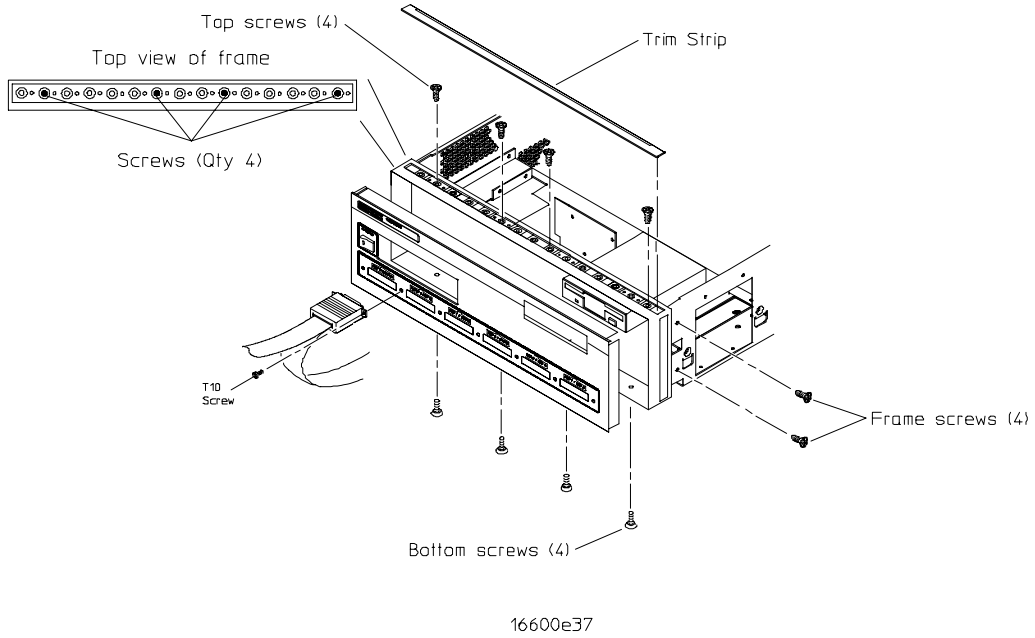
2 Using a Torx T10 screwdriver, remove the screws that secure the probe cables to the front panel of the instrument.

3 Remove the trim strip from the top of the front frame.

4 Using a Torx T15 screwdriver, remove four screws that secure the front panel to the front frame on the bottom of the frame.



5 Using a Torx T15 screwdriver, remove four screws that secure the front panel to the front frame on the top of the frame.



6 Remove the front panel from the frame.

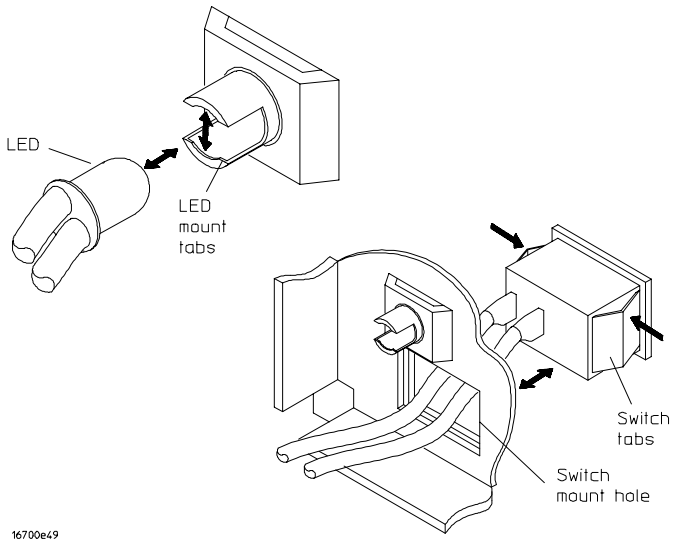
7 If necessary, remove the front frame from the deck.
   - **a** Using a Torx T15 screwdriver, remove four screws on the bottom of the front frame that secure the frame to the deck.
   - **b** Using a Torx T15 screwdriver, remove four screws, two on each side of the deck, that secure the front frame to the sides of the deck.
   - **c** Remove the front frame from the deck.

8 Reverse this procedure to install the front panel and front frame.

To remove and replace the line switch assembly

Both the line switch and power indicator LED are removed and replaced as a single assembly.

1. Using previous procedures, remove the following assemblies:
   - Cover
   - Front Panel
2. Disconnect the line switch cable from the acquisition board J9.
3. Using a 1/8-inch flat blade screwdriver, gently spread apart the tabs that hold the LED to the LED mount and pull the power indicator LED toward the rear of the instrument.
4. Using a 1/8-inch flat blade screwdriver, push against the line switch mount tabs while pushing the line switch out the front of the instrument.
5. Feed the cable through the line switch mounting hole.



6. Reverse this procedure to install the line switch assembly

   When installing the line switch assembly, the line switch is inserted in the front panel with the "0" to the left (that is, outboard).

To remove and replace a probe cable

1. Using a Torx T10 screwdriver, remove two screws that secure the probe cable to the front panel.
2. Unplug the probe cable from the front panel and remove the cable.
3. Reverse this procedure to install the probe cable.

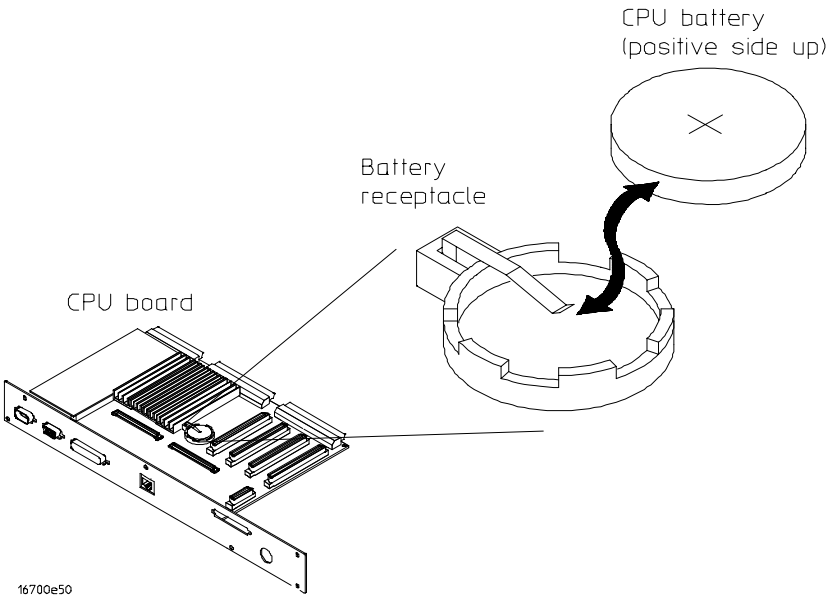
To remove and replace the CPU battery

1 Using previous procedures, remove the following assemblies:

- Top cover

2 Using a 1/8-inch flat blade screwdriver, gently pry the battery from the battery receptacle.

To prevent loss of data in the stable storage, remove and replace the battery as quickly as possible.



3 Insert a new battery (Panasonic BR2325 or equivalent) in the battery receptacle.

4 Reinstall the top cover.

Catastrophic Failure Recovery

The following procedures are performed after replacing

- CPU Board
- Hard Disk Drive

Note that these procedures are only required the first time the instrument is turned on after the failure and replacement.

To recover from a CPU board failure

1 After reassembling the instrument, connect the monitor, keyboard, and mouse to their rear panel ports.

2 Connect the power cord to the instrument and apply power to the instrument.

3 The monitor selection mode will be automatically enabled. Wait until until the monitor is readable and the monitor resolution displayed matches the actual resolution of the monitor. Press the [ENTER] key, then answer "Y" at the query.

4 When the boot process auto-terminates, type in the following commands at the Main Menu: Enter Command > prompt exactly as they appear (CAPS indicate command abbreviations):

```
MAin                            [ ENTER ]
COnfiguration AUto BOot ON      [ ENTER ]
COnfiguration AUto SEArch OFF   [ ENTER ]
COnfiguration BootTimer 0       [ ENTER ]
COnfiguration FastBoot OFF      [ ENTER ]
COnfiguration SECure OFF        [ ENTER ]
```

5 At the Main Menu: Enter Command prompt, type in the Boot command:

```
BOOT    [ ENTER ]
```

When the Boot command is entered, the instrument will complete the boot process.

To recover from a hard disk drive failure

1 After replacing the hard disk drive, reassemble the instrument.

2 Go to Reignite: Reloading the operating system in Chapter 5 to reinstall the operating system.

Returning Assemblies

Before shipping the logic analysis system or assemblies to Agilent Technologies, contact Agilent. In the United States, call 1-800-403-0801. Outside the United States, call your nearest Agilent Technologies Sales Office for additional details. Ask the Sales Office for the address of the nearest Agilent Technologies Service Center.

1 Write the following information on a tag and attach it to the part to be returned.

- Name and address of owner
- Model number
- Serial number
- Description of service required or failure indications

2 Remove accessories from the logic analysis system.

Only return accessories to Agilent Technologies if they are associated with the failure symptoms.

3 Package the logic analysis system or assemblies.

You can use either the original shipping containers, or order materials from an Agilent Technologies sales office.

CAUTION

For protection against electrostatic discharge, package the logic analyzer in electrostatic material.

4 Seal the shipping container securely, and mark it FRAGILE.

7

Replaceable Parts

Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your logic analysis system.

Replaceable parts ordering

Parts listed

To order a part on the list of replaceable parts, quote the Agilent Technologies part number, indicate the quantity desired, and address the order to the nearest Agilent Technologies Sales Office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Agilent Technologies Sales Office.

Direct mail order system

Within the USA, Agilent Technologies can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the Agilent Technologies Part Center. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Agilent Technologies Sales Office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and there are no invoices.

In order for Agilent Technologies to provide these advantages, a check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Agilent Technologies Sales Office. Addresses and telephone numbers are located in a separate document at the back of the Service Guide.

Exchange assemblies

Some assemblies are part of an exchange program with Agilent Technologies. The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Agilent Technologies.

After you receive the exchange assembly, return the defective assembly to Agilent Technologies. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Agilent Technologies will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Agilent Technologies Sales Office for information.

See Also "To return assemblies" in chapter 6.

Replaceable parts list description

The replaceable parts list is organized by reference designation.
The exploded view does not show all of the parts in the replaceable parts list.

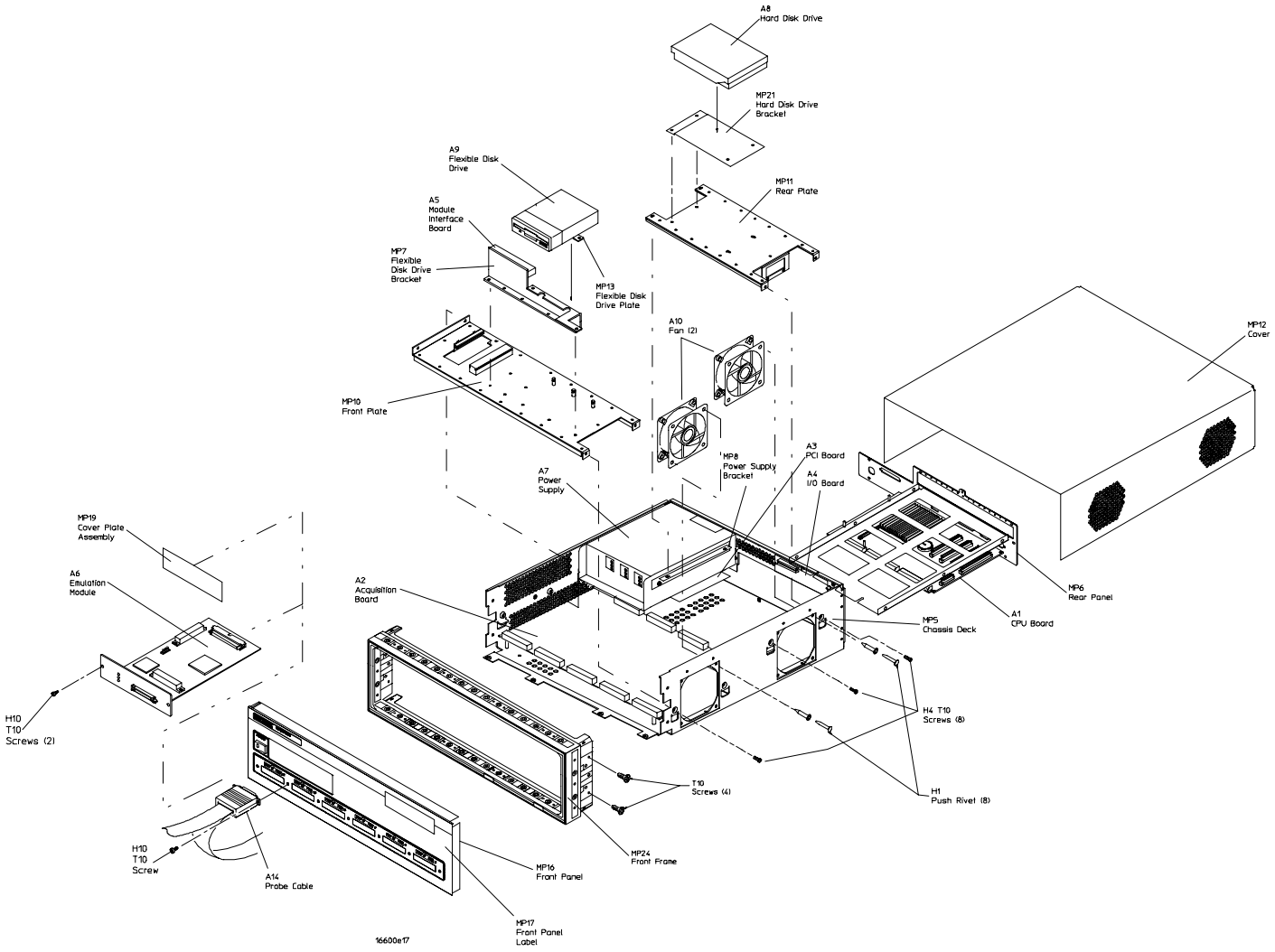
Information included for each part on the list consists of the following:

- Reference designator
- Agilent Technologies part number
- Total quantity included with the instrument (Qty)
- Description of the part

Reference designators used in the parts list are as follows:

- A Assembly
- E Miscellaneous Electrical Part
- F Fuse
- H Hardware
- MP Mechanical Part
- W Cable

16600A-series exploded view and replaceable parts



Exploded view of the 16600A-series

16600A-series Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
Exchange Assemblies			
A1	16600-69517		Exchange CPU Board
A2	16600-69502		Exchange Acquisition Board (16600A)
A2	16600-69503		Exchange Acquisition Board (16601A)
A2	16600-69504		Exchange Acquisition Board (16602A)
A2	16600-69505		Exchange Acquisition Board (16603A)
A3	16600-66501		Exchange PCI Board
A7	16600-69500		Exchange Power Supply
Replacement Assemblies			
A1	5063-1648	1	CPU Board
A2	16600-66502	1	Acquisition Board (16600A)
A2	16600-66503	1	Acquisition Board (16601A)
A2	16600-66504	1	Acquisition Board (16602A)
A2	16600-66505	1	Acquisition Board (16603A)
A3	16600-66501	1	PCI Board
A4	16600-66507	1	I/O Board
A5	16600-66508	1	Module Interface Board
A6	16600-66515	0	Run Control Board (optional)
A7	0950-2692	1	Power Supply
A8	0950-2811	1	Hard Disk Drive - 4GB
A9	0950-3251	1	Flexible Disk Drive
A10	3160-0818	2	Fan
A11	C3757-60401	1	Keyboard
A12	C4728-60101	1	Mouse - 3 button
A13	01650-61608	2	Probe Tip Assy
A14	01660-61605	6	Probe Cable (16600A)
A14	01660-61605	4	Probe Cable (16601A)
A14	01660-61605	3	Probe Cable (16602A)
A14	01660-61605	2	Probe Cable (16603A)
E1	5959-9333		Replacement probe leads (5 per package)
E2	5959-9334		Replacement probe grounds (5 per package)
E3	5959-9335		Replacement pod ground (2 per package)
E4	5090-4356		Grabber kit assembly (20 grabbers per package)
H1	0361-1787	8	Round Head Push Rivet (fan to deck)
H2	0380-1858	6	Jackscrew with Lock (RS-232-C, Monitor, and Parallel Printer ports to CPU rear panel)
H3	0380-4628	2	Hex Standoff (Acquisition board to chassis deck)
H4	0515-0372	39	M3.0 X 0.50 8mm T10 PH (Acquisition board to chassis deck, rear panel to chassis deck, I/O board to chassis deck, cover to chassis deck, module interface board to fdd bracket, PCI board to standoffs, rear plate to chassis deck, front plate to chassis deck, power supply to chassis deck rear, flexible disk drive plate to flexible disk drive bracket, board guide to front plate, flexible disk drive bracket to front plate)
H5	0515-0430	2	M3.0 X 0.50 6mm T10 PH (hard disk drive assy to rear plate)
H6	0515-1269	12	M4.0 X 0.70 10mm T15 90 deg FH (front panel frame to chassis deck, front panel to front panel frame)
H7	0515-1363	4	M3.0 X 0.50 5mm T10 Truss Head (flexible disk drive to flexible disk drive plate)
H8	0515-1403	8	M4.0 X 0.70 6mm T15 90 deg FH (chassis deck side to front panel frame, accessory pouch to cover)
H9	0515-2143	4	M4.0 X 0.70 6mm T15 PH (power supply bracket to power supply, accessory pouch to cover)
H10	0515-2998	9	M3.0 X 0.50 10mm LG (16600A, Emulation module or cover plate to front panel, probe mounting bracket to front panel
H10	0515-2998	7	M3.0 X 0.50 10mm LG (16601A, Emulation module or cover plate to front panel, probe mounting bracket to front panel

16600A-series Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
H10	0515-2998	6	M3.0 X 0.50 10mm LG (16602A, Emulation module or cover plate to front panel, probe mounting bracket to front panel
H10	0515-2998	5	M3.0 X 0.50 10mm LG (16603A, Emulation module or cover plate to front panel, probe mounting bracket to front panel
H11	1250-2075	1	9/16 in hex; 1/2-28 UNEF; 2B Threads;0.95 in thick; Ni plated brass (LAN BNC)
H12	1252-5828	1	Jack Screw Kit (SCSI connector)
H13	2360-0462	4	6-32 0.250 in T15 PH with washer)hard disk drive to hard disk drive bracket)
MP1	1400-2224	1	Cable Clamp
MP2	1400-2225	1	Cable Clamp
MP3	1450-0625	1	LED Retainer
MP4	01660-09101	6	Ground Spring (16600A)
MP4	01660-09101	4	Ground Spring (16601A)
MP4	01660-09101	3	Ground Spring (16602A)
MP4	01660-09101	2	Ground Spring (16603A)
MP5	16600-00101	1	Chassis Deck
MP6	16600-00206	1	Rear Panel
MP7	16600-01201	1	Flexible Disk Drive Bracket
MP8	16600-01203	1	Power Supply Bracket
MP9	16600-01205	1	Probe Mounting Bracket (16600A)
MP9	16601-01201	1	Probe Mounting Bracket (16601A)
MP9	16602-01201	1	Probe Mounting Bracket (16602A)
MP9	16603-01201	1	Probe Mounting Bracket (16603A)
MP10	16600-04101	1	Front Plate
MP11	16600-04102	1	Rear Plate
MP12	16600-04103	1	Cover
MP13	16600-04104	1	Flexible Disk Drive Plate
MP14	16600-23101	1	Board Guide
MP15	16600-25401	1	Insulator
MP16	16600-60201	1	Front Panel (16600A)
MP16	16601-60201	1	Front Panel (16601A)
MP16	16602-60201	1	Front Panel (16602A)
MP16	16603-60201	1	Front Panel (16603A)
MP17	16600-94301	1	Front Panel Label (16600A)
MP17	16601-94301	1	Front Panel Label (16601A)
MP17	16602-94301	1	Front Panel Label (16602A)
MP17	16603-94301	1	Front Panel Label (16603A)
MP18	16600-94302	1	ID Label (16600A)
MP18	16601-94302	1	ID Label (16601A)
MP18	16602-94302	1	ID Label (16602A)
MP18	16603-94302	1	ID Label (16603A)
MP19	16600-68708	1	Cover Plate Assembly (includes label)
	- 16600-04105		Cover Plate
	- 16600-94304		Label - Blank
MP20	16600-94310	1	Label - Probe and Cable
MP21	16700-01202	1	Hard Disk Drive Bracket
MP22	16700-84501	1	Accessory Pouch
MP23	35672-21703	2	Retainer Strap
MP24	5022-1188	1	Front Frame
MP25	5041-9171	2	Side Trim
MP26	5041-9176	1	Top Trim
MP27	5090-4370	1	Label - Stock
MP28	54810-44901	1	Molded Handle
MP29	54810-45001	2	Handle End Cap
MP30	8160-1226	16	RFI Spring (Front Panel)
MP31	8160-1227	6	Spring (Flexible Disk Drive plate)
MP32	0363-0125		RFI Spring (two 75mm sections, side of chassis deck at front)
MP33	0460-2010		Foam Tape (25mm, flexible disk drive data cable to top of flexible disk drive)

16600A-series Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
W1	16600-61601	1	Cable - Keyboard/Mouse
W2	16600-61602	1	Cable - Power Sense
W3	16600-61603	1	Cable - Flexible Disk Drive Data
W4	16600-61604	1	Cable - Flexible Disk Drive Power
W5	16600-61605	1	Cable - Fan
W6	16600-61606	1	Cable - Line Switch (includes line switch and power indicator LED)
W7	16600-61607	1	Cable - Auxiliary Power
W8	16600-61609	1	Cable - Hard Disk Drive Data
W9	16600-61610	1	Cable - Measurement Module
W10	16600-61611	1	Cable - Hard Disk Drive Power
W11	16500-61621	1	Cable - Target Control
	16500-40502	1	Filler Panel Assembly
	16600-14600	1	CD-ROM Drive
W16	8120-1521	1	Power cord - United States (7.5 ft)
W16	8120-1703	1	Power cord (Option 900-UK)
W16	8120-0696	1	Power cord (Option 901-Austl)
W16	8120-1692	1	Power cord (Option 902-Eur)
W16	8120-2296	1	Power cord (Option 906-Swit)
W16	8120-2957	1	Power cord (Option 912-Den)
W16	8120-4600	1	Power cord (Option 917-Africa)
W16	8120-4754	1	Power cord (Option 918-Japan)
W16	8120-8377	1	Power cord (Option 922-China)

8

Theory of Operation

Theory of Operation

This chapter tells the theory of operation for the logic analysis system and describes the self-tests. The information in this chapter is to help you understand how the logic analysis system operates and what the self-tests are testing. This information is not intended for component-level repair.

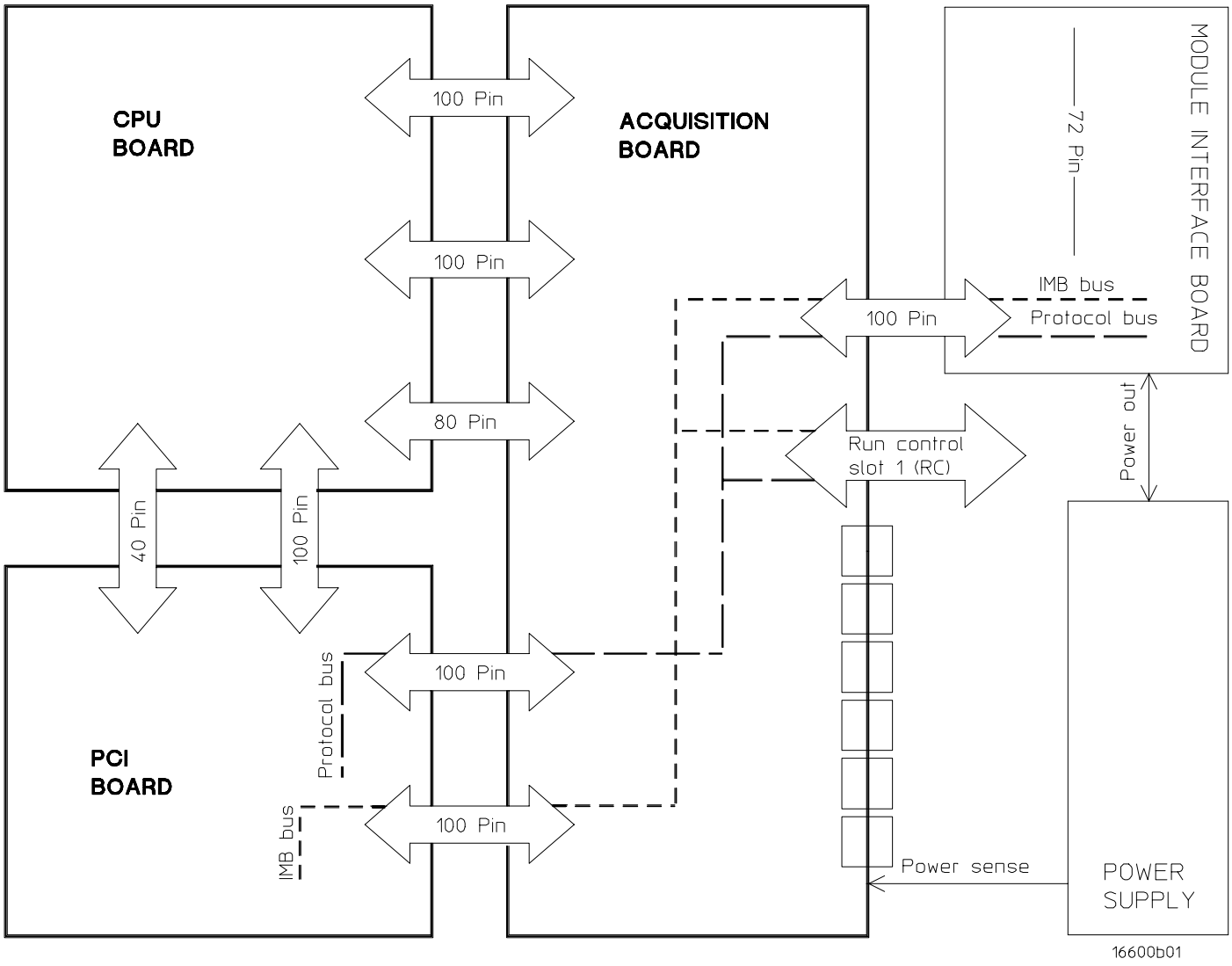
Block-Level Theory

The block level theory includes the theory of operation of the 16600A-series Logic Analysis System in terms of the major subsystems.

The 16600A-series Logic Analysis System

The system level block diagram is shown on the following page. It includes the following subsystems:

- CPU board
- PCI board
- Acquisition board
- Measurement module backplane
- Emulation module interface
- Power supply



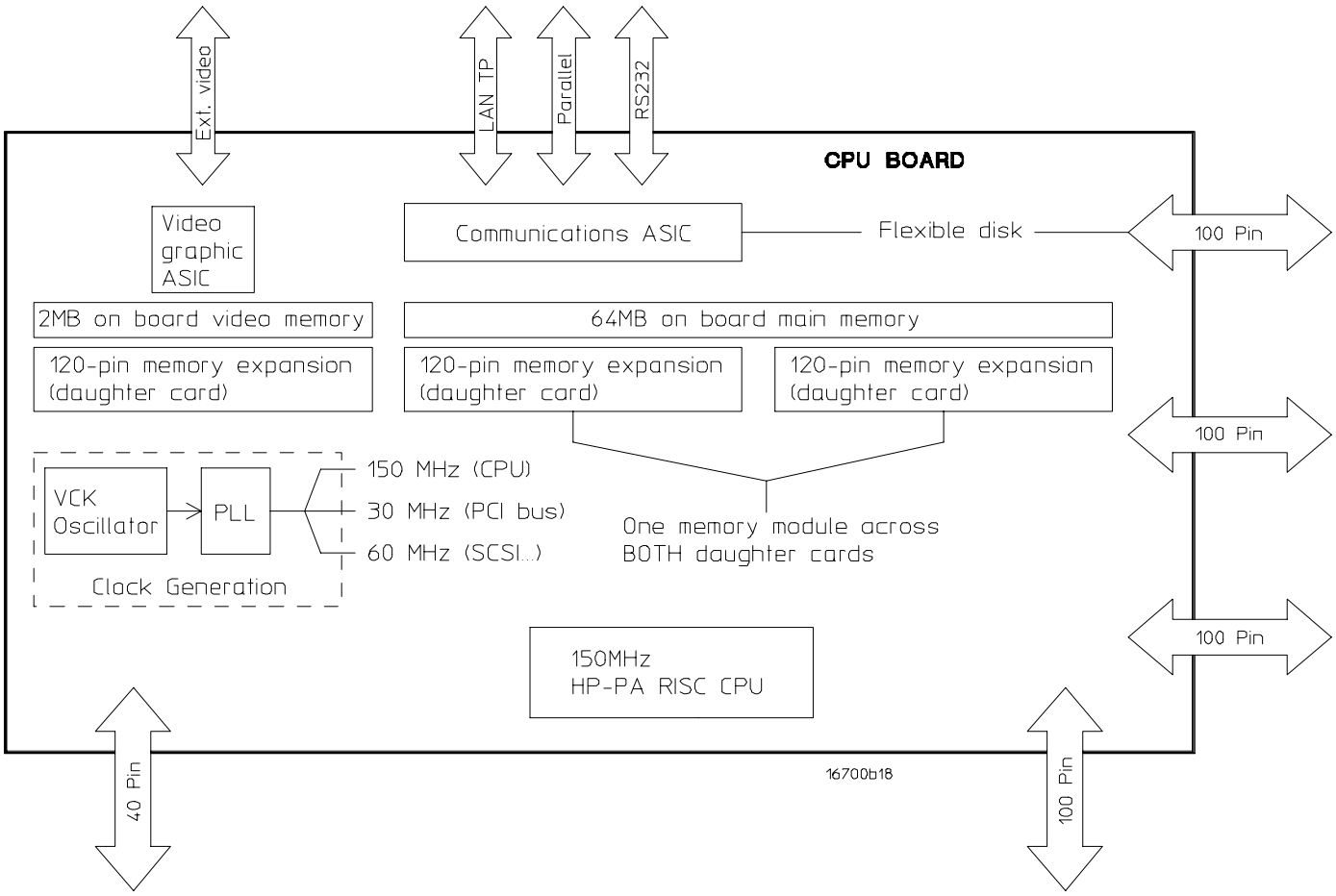
The Logic Analysis System

Subsystem overview theory

The following is a discussion of the subsystems and the components that make up each subsystem.

CPU board

The CPU is a 150-MHz PA-RISC workstation processor. The CPU board, working with both the PCI board and interface board, manages the data flow between the mainframe components and both the measurement modules and emulation modules.



The CPU Board

The CPU is supported by the following components:

Clock Circuitry A 30-MHz on-board crystal oscillator is on the CPU board. The 30-MHz frequency is divided by 2, then upconverted by a PLL clock-distribution IC to also create 60 MHz and 150 MHz. The 15 MHz, 30 MHz, and 60 MHz frequencies are utilized by buses and backplanes. The 150 MHz frequency is utilized by the processor.

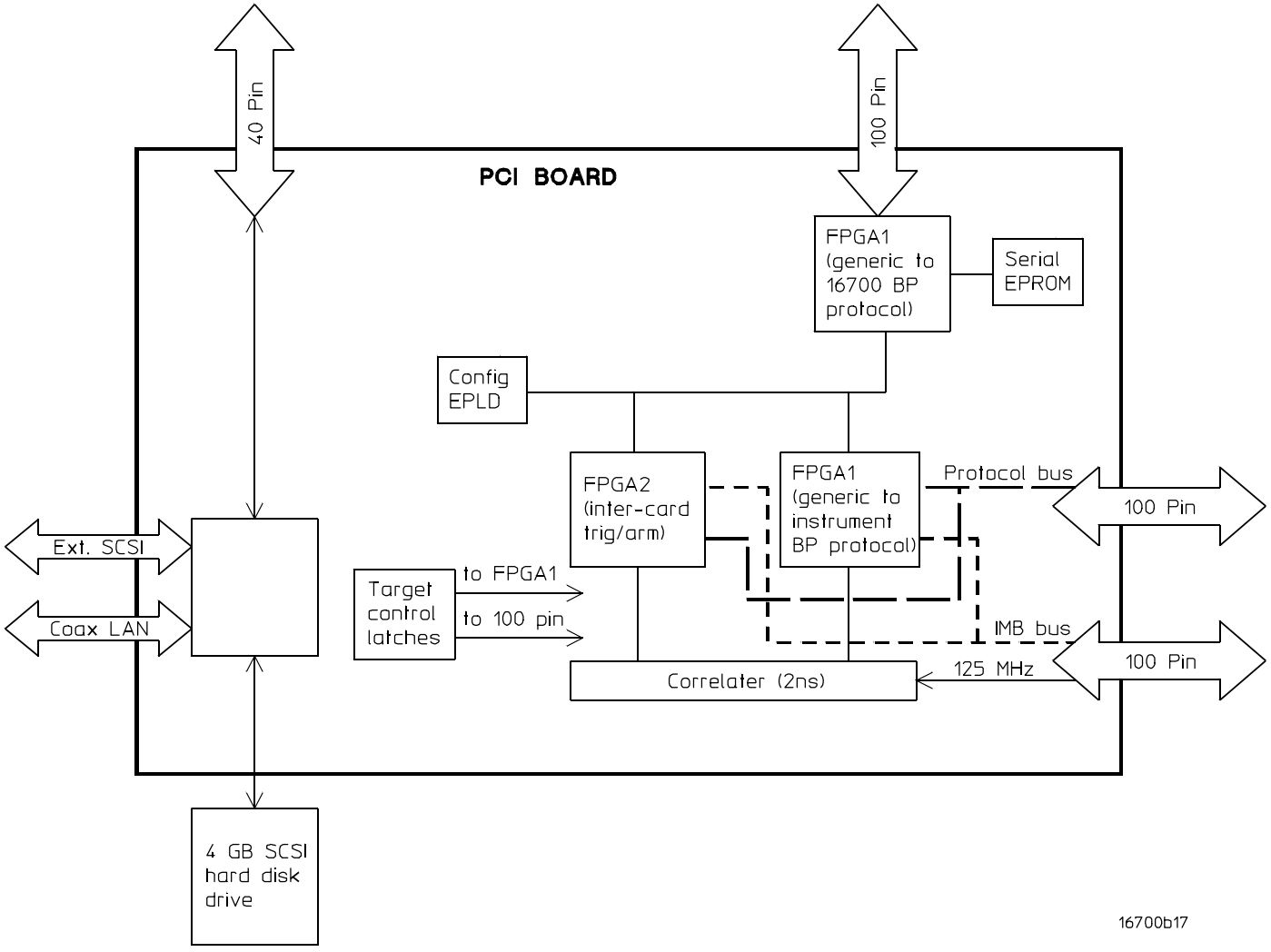
System RAM A total of 64 MB of system RAM is available in the factory default configuration. 32 MB of base on-board system memory is present, plus a 32 MB proprietary memory daughter card is added.

I/O Most of the I/O ports are directly managed by the CPU board. These include the LAN (10BaseT twisted pair), PS/2, RS-232-C, Centronics, flexible disk drive, and the display. Proprietary ASICs are used as device interfaces to the I/O components.

Graphics The Graphics, or display, is implemented by a proprietary graphics accelerator ASIC supported by 2 MB of synchronous graphics RAM. The graphics ASIC has two video outputs. One video output is an RBG signal routed to the I/O board. The second video output is a digital video signal which is routed to a connector on the CPU board. The digital video signal is only utilized by the Agilent Technologies 16702A mainframe flat panel display.

PCI board

The PCI board bridges the PCI backplane of the CPU board to an instrument backplane that interfaces with the measurement modules. Instrument backplane control is managed by the PCI board.



The PCI Board

PCI control functionality includes:

- Intermodule bus (IMB) with fixed and mixed trigger event inputs, module ARM, and port in/out
- 2 ns data time correlation across measurement modules
- Intermodule signaling bus
- Interframe signaling bus
- Target control bus
- Synchronous module data acquisition

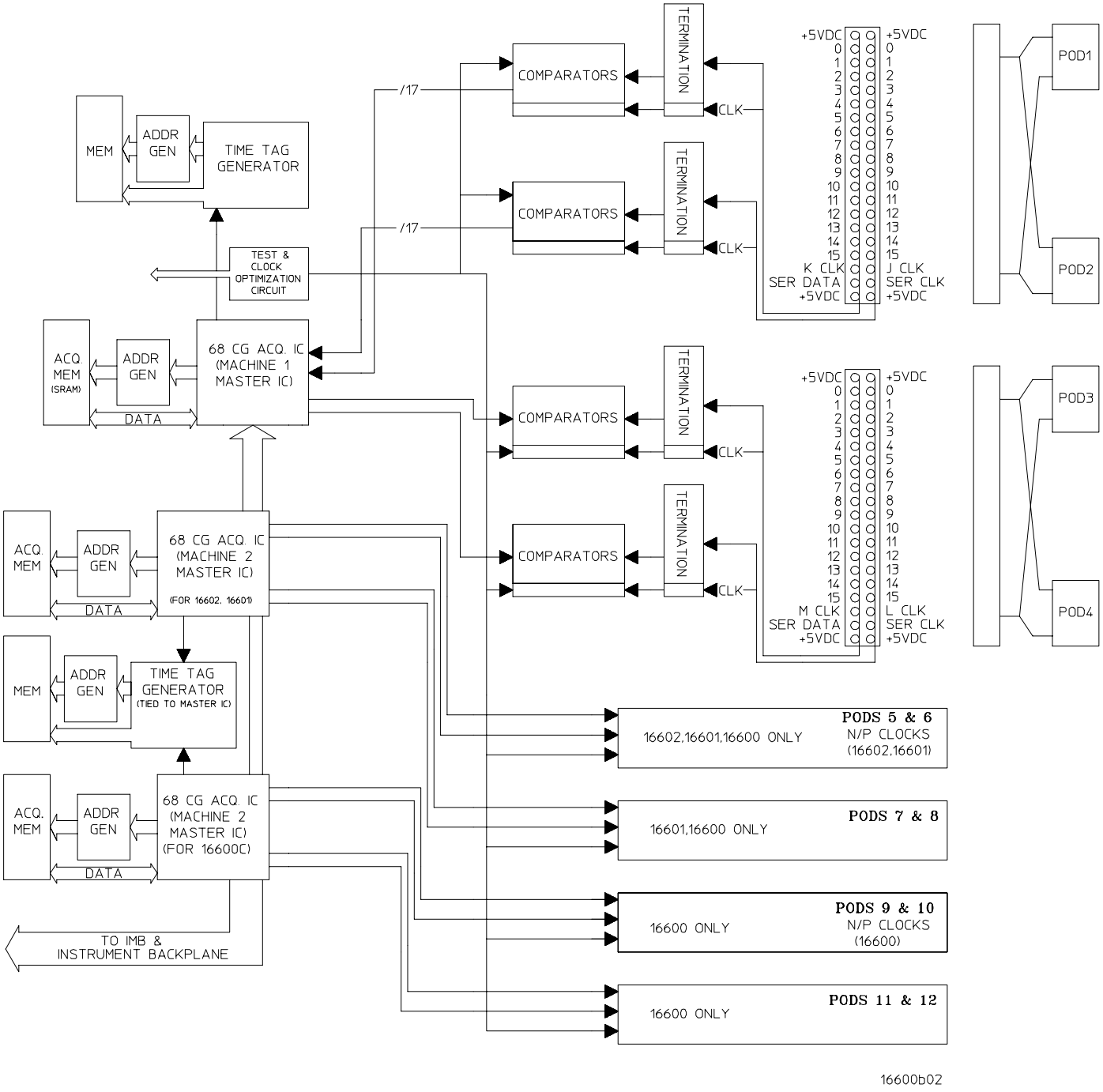
Additionally, the PCI board provides I/O port capability that is not available on the CPU board. The I/O port capability is extended to the I/O board. I/O port capability includes:

- External single-ended SCSI
- Internal SCSI
- LAN (10Base2)
- Port In/Out

Because it is the interface between the CPU and the instrument measurement front end, the PCI board hardware is suspect in the event the PV software (Self-Test) fails to load when initiated.

Acquisition board

The acquisition board provides all circuitry for acquiring, conditioning, processing, and distributing samples.



The Acquisition Board

Probing The probing circuit includes the probe cable and terminations. The probe cable consists of two 17-channel pods which are connected to the circuit board using a high-density connector. Each pod passes 16 single-ended data channels and one single-ended clock/data channel to the circuit board. If the clock/data channel is not used as a state clock in state acquisition mode, it is available as a data channel. The clock/data channel is also available as a data channel in timing acquisition mode.

The cables utilize nichrome wire woven in polyarmid yarn for reliability and durability. The pods also include one ground path per channel in addition to a pod ground. The channel grounds are configured such that their electrical distance is the same as the electrical distance of the channel. The probe tip assemblies and termination modules connected at the end of the probe cables have a divide-by-10 RC network which reduces the amplitude of the data signals as seen by the circuit board. This adds flexibility to the types of signals the circuit board can read in addition to improving signal integrity.

The terminations on the circuit board are resistive terminations, which reduce transmission line effects on the cable. The terminations also improve signal integrity to the comparators by matching the impedance of the probe cable channels with the impedance of the signal paths of the circuit board. All 17 channels of each pod are terminated in the same way. The signals are still reduced by a factor of 10.

Comparators Two proprietary 9-channel comparators interpret the incoming data and clock signals as either high or low, depending on where the user-programmable threshold is set. The threshold voltage of each pod is individually programmed, and the voltage selected applies to the clock channel as well as the data channels of each pod.

Each of the comparator ICs has a serial test input port used for testing purposes. A test bit pattern is sent from the Test and Clock Synchronization Circuit to the comparator. The comparators then propagate the test signal on each of the nine channels of the comparator. Consequently, all data and clock channel pipelines on the circuit board can be tested by the operating system software from the comparator.

Acquisition The acquisition circuit is made up of an Agilent Technologies proprietary ASIC. All of the sequencing, pattern/range recognition, and event counting functions are performed on board the IC.

In addition to the storage qualification and counting functions, the acquisition ASICs also perform master clocking functions. All state acquisition clocks are fed to each IC, and the ICs generate their own sample clocks. Every time the user selects RUN, the ICs individually perform a clock optimization before data is stored. Clock optimization involves using programmable delays on board the IC to position the master clock transition where valid data is captured. This procedure greatly reduces the effects of channel-to-channel skew and other propagation delays.

In the timing acquisition mode an oscillator-driven clock circuit provides a four-phase 100 MHz clock signal to each of the acquisition ICs. For high speed timing acquisition (100 MHz and faster) the sample period is determined by the four-phase 100 MHz clock signal. For slower sample rates, one of the three acquisition ICs divides the 100 MHz clock signal to the appropriate sample rate. The sample clock is then fed to all three acquisition ICs.

Threshold A precision octal DAC and precision op amp drivers comprise the threshold circuit. The DAC has individually programmable channels which allows the user to set the thresholds of the individual pods. The 16 data channels and the clock channel of each pod are all set to the same threshold voltage.

Test and Clock Synchronization Circuit ECLinPS (TM) ICs are utilized in the Test and Clock Synchronization Circuit for reliability and low channel-to-channel skew. Test patterns are generated and sent to the comparators during software operation verification. The test patterns are propagated across all data and clock channels and read by the acquisition ASIC to ensure both the data and clock pipelines are operating correctly.

The Test and Clock Synchronization Circuit also generates a four-phase 100 MHz sample/synchronization signal for the acquisition ICs operating in the timing acquisition mode. The synchronizing signal keeps the internal clocking of the individual acquisition ASICs in lock-step with the other ASICs in the 16600A-series instrument at fast sample rates. At slower sample rates, one of the acquisition ICs divides the 100 MHz clock signal to the appropriate sample rate. The slow speed sample clock is then utilized by all three acquisition ICs.

+5VDC supply The +5VDC supply circuit supplies power to active logic analyzer accessories such as analysis probes. LC filtering is utilized to ensure the power is clean. Thermisters on both the +5VDC supply lines and the ground return line protect both the 16600A-series instrument and the active accessory from overcurrent conditions. When an overcurrent condition is sensed, the thermisters create an open which shuts off the current from the +5VDC supply. After a reset time of approximately 20 seconds, the thermister closes the circuit and makes the supply current available.

Additional system support functionality The acquisition board also distributes most of the signals from both the CPU board and the PCI board throughout the system. Additionally, the acquisition board provides additional functionality not found on either the CPU or PCI board.

The acquisition board includes circuitry to synchronize the 100-MHz backplane module sample clock with the 500 MHz sample correlation clock to improve sample time correlation.

Measurement module backplane

The measurement module backplane is the same backplane used in the Agilent Technologies 16500-series logic analysis system. Consequently most of the 16500-series modules existing at the time of the 16600A- and 16700A-series releases will operate in those mainframes. Additional enhancements are also present to accommodate newer 16700A-series modules. Enhancements include a common sample clock to improve measurement time correlation and an optional handshaked transfer and 16-bit multiplexed address/data bus transfer to speed data transfer from the modules to system memory.

Emulation module interface

Processor run control, provided by the emulation module, is used to control the target system processor execution and allow access to target system resources. Target system processors viable for use with the emulation module include some form of N-wire control. Access to the emulation module is through the mainframe interface.

The emulation module is a Motorola 68332 system. The 68332 processor is used to control the N-wire and JTAG protocols for the target system processor.

The emulation module physically resides on the measurement module backplane. Communications between the mainframe CPU and the emulation module is managed by a run control server on the CPU board. The server manages the interrupts to and communications with the 68332 processor on the emulation module. Memory-mapped I/O allows the CPU to communicate with the module for data transfers.

Power supply

The power supply provides all power to the logic analysis system. The input voltage is autoselecting with respect to both voltage and frequency. The DC output voltage provided includes -12 V, -5.2 V, -3.25 V, +3.4 V, +5.1 V, and +12 V. The mainframe itself consumes 100 W of power. Each measurement module has an 80 W power budget, and each emulation module has a 25 W power budget. Maximum power consumed in a fully loaded mainframe is 600 W.

Power control

The front panel power switch does not directly control the line voltage. The power switch manages a control circuit through the CPU. When power is applied, the control circuitry immediately responds to input from the power switch. When the instrument is turned off without initiating a shutdown, the power switch asserts an interrupt to the CPU. The CPU then begins system cleanup in preparation for powerdown. When system cleanup is completed, the instrument then powers down.

Note that if the front panel switch is disconnected from the interface board, the instrument will never power down.

Power sense

The power sense circuitry, managed by the CPU, directly controls the state of the power supply. A control signal is directed to the power supply through the power sense cable. When the control signal is asserted, the power supply will activate. The power supply will then deactivate when the control signal is deasserted.

Note that if the power sense cable is disconnected from the interface board, the instrument will never power up.

When power is applied to the 16600A-series Logic Analysis System, a series of tasks called the power-up routine is performed to initialize and to verify operation of the mainframe. The mainframe display reports the progress and status of the power-up routine. Each of the tasks of the power-up routine is scrolled onto the mainframe display as the task is being performed.

The following is a complete listing of the power-up routine dialogue (or boot dialogue). The parts of the power-up routine dialogue are then discussed. Some of the details may vary slightly depending on the firmware revisions.

```
Firmware Version  1.1
Simple Console IO Dependent Code [IODC] Revision 1
Memory Test/Initialization Completed

To select a new Graphics Monitor Type press the [TAB] key now, otherwise EXIT
by entering any other key (or will time out in 15 seconds)...

(c) Copyright 1995-1998, Hewlett-Packard Company, All rights reserved
  Processor   Speed            State           Coprocessor State  Cache Size
  ---------  --------   ---------------------  -----------------  ----------
      0      150 MHz    Active                 Functional          64 KB
  Available memory (bytes)    :  67108864
  Good memory required (bytes):  67108864
  Primary boot path:    SESCSI.6.0
  Alternate boot path:  SESCSI.1.0
  Console path:         GRAPHICS(0)
  Keyboard path:        PS2

Processor is booting from first available device.
To discontinue, press any key within 2 seconds.
2 seconds expired.
Proceeding...
Trying Primary Boot Path
------------------------
Booting...
BOOT IO Dependent Code (IODC) revision 153

HARD Booted.
ISL Revision A.00.38  OCT 26, 1994
ISL booting  hpux
boot
 disk(8/16/5.6.0.0.0.0.0;0)/stand/vmunix
 3526196 + 315392 + 298272 start 0x192368
vuseg=a13000
 inet_site:ok  inet_cots:ok starship_attach: vendor id=103c, device id=1650
    System Console is on the ITE
Networking memory for fragment reassembly is restricted to 5378040 bytes
Logical volume 64, 0x3 configured as ROOT
Logical volume 64, 0x2 configured as SWAP
Logical volume 64, 0x2 configured as DUMP
   Swap device table:  (start & size given in 512-byte blocks)
       entry 0 - major is 64, minor is 0x2; start = 0, size = 1540096
Checking root file system.
```

```
File system is clean - log replay is not required
Rook check done.
Starting the STREAMS daemons.
   B23528 HP-UX (B.10.20) #1 Sun Jun  9 08:03:38 PDT 1996
Memory Information
   physical: page size = 4096 bytes, logical page size = 4096 bytes
   Physical: 65536 Kbytes, lockable: 39088 Kbytes, available 47856 Kbytes
/abin/ioinitrc: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             #     # #               #######   ####    ####     #    ####
                                Logic Analysis System


/sbin/bcheckrc:
Checking for LVM volume groups and Activating (if any exist)
Volume group '/dev/vg00' has been successfully changed.
vxfa fsck: sanity check: root file system OK (mounted read/write)
/sbin/itemap: WARNING! An attempt to write keyboard mapping entries past
/sbin/itemap: the end of the buffer.  Further writes will be ignored.
Checking hfs file systems /sbin/fsclean:
/dev/vg00/lvell (mounted) ok
HFS file systems are OK, not running fsck
Checking vxfs file systems
/dev/vg00/lvol3 :
vxfa fsck: sanity check: root file system OK (mounted read/write)
/dev/vg00/lvol4 :
vxfa fsck: sanity check: /dev/vg00/lvol4 OK
```

```
/dev/vg00/lvol5 :
vxfa fsck: sanity check: /dev/vg00/lvol5 OK
/sbin/auto_parms, checking network for DHCP server (see /etc/autoparms.log)
     HP-UX Start-up in progress                      Status
     ___________________________                     ______

     Mount file systems ........................... [ OK ]
     Setting hostname ............................. [ OK ]
     Enable auxiliary swap space .................. [ OK ]
     Start syncer daemon .......................... [ OK ]
     Configure LAN interfaces ..................... [ OK ]
     Start Software Distributor agent daemon ...... [ OK ]
     Clean up old log files ....................... [ OK ]
     Start system message logging daemon .......... [ OK ]
     Configure HP Ethernet interfaces ............. [ OK ]
     Configure LAN interfaces ..................... [ OK ]
     Start NFS core subsystem ..................... [ OK ]
     Start NFS client subsystem ................... [ OK ]
     Start Internet services daemon ............... [ OK ]
     Start time synchronization ................... [N/A ]
     Start print spooler .......................... [ OK ]
     Start clock daemon ........................... [ OK ]
     Set X11 Device Configuration ................. [ OK ]
     Start HP16700 Processor Run Control daemon .... [ OK ]
     Start NFS server subsystem ................... [ OK ]
     Start Lngrd daemon ........................... [ OK ]

The system is ready.
Starting HP Logic Analysis System ...
```

Booting from the boot ROM - processor dependent code (pdc)

The following segment of the boot dialogue is created by the boot ROM. The boot ROM is managing the boot process during this stage of the power-up routine.

```
Firmware Version  1.1
Simple Console IO Dependent Code [IODC] Revision 1
Memory Test/Initialization Completed


To select a new Graphics Monitor Type press the [TAB] key now, otherwise EXIT
by entering any other key (or will time out in 15 seconds)...


-------------------------------------------------------------------------------
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-------------------------------------------------------------------------------
  Processor   Speed            State           Coprocessor State  Cache Size
  ---------  --------   --------------------  -----------------  ----------
      0      150 MHz    Active                Functional          64 KB
  Available memory (bytes)    :  67108864
  Good memory required (bytes):  67108864

  Primary boot path:    SESCSI.6.0
  Alternate boot path:  SESCSI.1.0
  Console path:         GRAPHICS(0)
  Keyboard path:        PS2
Processor is booting from first available device.
To discontinue, press any key within 2 seconds.
```

```
2 seconds expired.
Proceeding...
Trying Primary Boot Path
------------------------
```

During the boot ROM stage of the power-up routine, the CPU board is first tested and the device path configuration is loaded. As part of the CPU board test, system RAM is tested. The following text shows the available system memory recognized by the boot ROM:

```
  Available memory (bytes)    :  67108864
  Good memory required (bytes):  67108864
```

The boot ROM then configures the device paths, tests the device at the primary boot path to see that it is a viable boot device, and then attempts to boot from the device. The device associated with the primary boot path is the hard disk drive.

```
  Primary boot path:    SESCSI.6.0
  Alternate boot path:  SESCSI.1.0
  Console path:         GRAPHICS(0)
  Keyboard path:        PS2
  Processor is booting from first available device.
```

Booting from the boot device - initial system loader (isl)

After the boot ROM stage of the power-up routine, the instrument will boot from the device at the primary boot path address, the hard disk drive. The hard disk drive is now managing the boot process during this stage of power-up.

```
Booting...
BOOT IO Dependent Code (IODC) revision 153


HARD Booted.
ISL Revision A.00.38  OCT 26, 1994
ISL booting  hpux
boot
  disk(8/16/5.6.0.0.0.0.0;0)/stand/vmunix
  3526196 + 315392 + 298272 start 0x192368
vuseg=a13000
  inet_site:ok  inet_cots:ok starship_attach: vendor id=103c, device id=1650


    System Console is on the ITE
Networking memory for fragment reassembly is restricted to 5378040 bytes
Logical volume 64, 0x3 configured as ROOT
Logical volume 64, 0x2 configured as SWAP
Logical volume 64, 0x2 configured as DUMP
   Swap device table:  (start & size given in 512-byte blocks)
       entry 0 - major is 64, minor is 0x2; start = 0, size = 1540096
Checking root file system.
File system is clean - log replay is not required
Rook check done.
Starting the STREAMS daemons.
   B23528 HP-UX (B.10.20) #1 Sun Jun  9 08:03:38 PDT 1996
Memory Information
   physical: page size = 4096 bytes, logical page size = 4096 bytes
   Physical: 65536 Kbytes, lockable: 39088 Kbytes, available 47856 Kbytes
/abin/ioinitrc:
```

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             #     # #               #        #    #  #    #    #   #    #
             #     # #               #######   ####    ####     #    ####
                                Logic Analysis System


/sbin/bcheckrc: Checking for LVM volume groups and Activating (if any exist)
Volume group '/dev/vg00' has been successfully changed.
vxfa fsck: sanity check: root file system OK (mounted read/write)
/sbin/itemap: WARNING! An attempt to write keyboard mapping entries past
/sbin/itemap: the end of the buffer.  Further writes will be ignored.
Checking hfs file systems /sbin/fsclean: /dev/vg00/lvell (mounted) ok
HFS file systems are OK, not running fsck
Checking vxfs file systems
/dev/vg00/lvol3 :
vxfa fsck: sanity check: root file system OK (mounted read/write)
/dev/vg00/lvol4 :
vxfa fsck: sanity check: /dev/vg00/lvol4 OK
/dev/vg00/lvol5 :
vxfa fsck: sanity check: /dev/vg00/lvol5 OK
/sbin/auto_parms, checking network for DHCP server (see /etc/autoparms.log)
```

When the `Booting...` message appears, the instrument is beginning to load the operating system, and the scope of power-up and configuration begins to move from just the CPU board to the subsystems on the instrument CPU backplane.

```
boot
 disk(8/16/5.6.0.0.0.0.0;0)/stand/vmunix
 3526196 + 315392 + 298272 start 0x192368
```

The operating system kernel, including device configurations, is being loaded into memory. This signifies that the CPU board, memory, and boot device are operational.

```
vuseg=a13000
 inet_site:ok  inet_cots:ok starship_attach: vendor id=103c, device id=1650
```

The PCI board has now been recognized, and the CPU now has a path to the CPU backplane and the system devices on the backplane.

The file system on the hard drive is then checked.

```
Checking root file system.
File system is clean - log replay is not required
```

If the system was previously powered-down abnormally, then the file system would include a journal file. The instrument would then replay the detected journal file in an attempt to recover the instrument state prior to the abnormal shutdown. During the remainder of the boot routine in this case, the text "Log replay in progress" appears repeatedly in the boot dialogue.

The system memory is again tested. If 64 MB of system memory was installed, the following message appears:

```
Memory Information
   physical: page size = 4096 bytes, logical page size = 4096 bytes
   Physical: 65536 Kbytes, lockable: 39088 Kbytes, available 47856 Kbytes
```

For the remainder of the isl boot stage, the file system is further checked. The devices on the backplane are also checked and configured.

Initialization

During initialization, all of the hardware subsystems and supporting software processes are initialized and started. Most failures at this point will be caused by software or configuration errors.

```
HP-UX Start-up in progress                    Status
______________________________                ______

Mount file systems ............................ [ OK ]
Setting hostname .............................. [ OK ]
Enable auxiliary swap space ................... [ OK ]
Start syncer daemon ........................... [ OK ]
Configure LAN interfaces ...................... [ OK ]
Start Software Distributor agent daemon ....... [ OK ]
Clean up old log files ........................ [ OK ]
Start system message logging daemon ........... [ OK ]
Configure HP Ethernet interfaces .............. [ OK ]
Configure LAN interfaces ...................... [ OK ]
Start NFS core subsystem ...................... [ OK ]
Start NFS client subsystem .................... [ OK ]
Start Internet services daemon ................ [ OK ]
Start time synchronization .................... [N/A ]
Start print spooler ........................... [ OK ]
Start clock daemon ............................ [ OK ]
Set X11 Device Configuration .................. [ OK ]
Start HP16700 Processor Run Control daemon .... [ OK ]
Start NFS server subsystem .................... [ OK ]
Start Lngrd daemon ............................ [ OK ]
```

Logic analysis system load

After the instrument core subsystems are tested and configured, the final stage of the power-up routine begins. During the final stage, the logic analysis system software is loaded. The logic analysis system software includes the mainframe and module software, and toolset licenses.

```
The system is ready. Starting HP Logic Analysis System ...
```

The CPU and the devices on the CPU backplane that form the infrastructure of the system are tested and are operational. Now the CPU polls the devices on the measurement module backplane. After reading the ID codes of the installed modules, the CPU then loads the appropriate measurement module software from the boot device into system memory. After the module software is downloaded into memory, the modules are initialized and calibration factors loaded (for modules requiring calibration factors from an operational accuracy calibration).

The session manager autolaunches, which in turn autolaunches a local logic analysis session. When the System window appears, the instrument is ready for use. Any module configuration errors appear in a status window when the System window is opened.

Self-Tests Description

Performance Verification, or Self-Test, is made up of a series of software routines that exercise instrument subsystems to verify that the subsystems are operational.

Performance Verification is performed at two levels: on boot, and using the performance verification software (PV software). The two levels of performance verification are designed to be complimentary. That is, if a subsystem is tested during boot, there will not be a user-initiated performance verification test in the PV software to operationally verify the same subsystem. Likewise, the PV software is designed to tests the operation of instrument subsystems that have not been tested on boot.

When the PV software is initiated by the user the measurement session is exited, discarding all measurement configurations. The user is warned of this prior to entering the PV software to give them the opportunity to cancel loading of the software. The measurement session is exited because the PV software tests leave the hardware in an unknown state. Restarting the measurement session after running the PV software is required to properly reinitialize the hardware to again run measurements.

Performance Verification on boot

During powerup, both the CPU and system memory are tested as part of the initial firmware execution. This occurs very early in the power up boot routine. After the CPU and memory tests are complete, the display will show that the firmware recognizes both the CPU and system memory.

When the memory has been tested and passes, the display will show the following message:

```
Memory Test/Initialization Completed
```

When the CPU has been tested and passes, the display will show the following report about the CPU:

```
Processor   Speed           State           Coprocessor State  Cache Size
---------  --------  ---------------------  -----------------  ----------
    0      150 MHz   Active                 Functional          64 KB
Available memory (bytes)    :  67108864
Good memory required (bytes):  67108864
```

This shows that 64 MB of system memory is installed and recognized by the boot ROM. If 160 MB of system memory is installed, then the number of available bytes would be 167772160. However, if the CPU system memory daughter card is not installed or not properly seated, then only the base 32 MB system memory would be recognized, and the boot dialogue would show only 33554432 bytes available.

The hard disk drive is then tested during this phase of the power up boot routines. During the initial firmware execution, the hard disk drive is searched for. When the hard disk drive is found, the display will report:

```
Trying Primary Boot Path
------------------------
Booting...
```

The instrument then attempts to boot from the hard disk drive. Operation of the hard disk drive is verified, after which the instrument loads the operating system. The following message is displayed when the operating system begins to load:

```
ISL booting  hpux
boot
  disk(8/16/5.6.0.0.0.0.0;0)/stand/vmunix
  3526196 + 315392 + 298272 start 0x192368
```

When the above message appears, it implies that the instrument central processor, system memory (RAM), and hard disk drive are operational. If any of these subsystems are not operational, an error message will appear and the boot process halted. Refer to the troubleshooting flowcharts for more information on boot errors.

Performance Verification using the PV software

The PV software (Self Test) provides additional confidence in the operation of the instrument by verifying subsystems that are not tested as part of the boot routines. The tests are divided between system tests and frame tests.

System tests

The system tests verify the operation of the logic analysis system core that have not been tested during power up boot routines. Verified during the System tests are the PCI board and parts of the CPU board not tested during boot.

When "Test All" is selected, some of the tests will not run and return a "Not Executed" status because operator action is required. These tests must be selected and run individually by the user. When the tests requiring user action are run, the user is prompted for the specific action that is needed for successful completion of the test. When the indicated user action is performed, and the tested subsystem is operational, the specific test will return a "Passed" status.

For the CPU board, the tests that require user action are:

Test:	User Action:
Floppy Drive Test	A DOS-formatted floppy must be in the drive
External SCSI Test	A powered-up CD-ROM drive must be on the bus
Parallel Port Test	A parallel port loop back connector must be installed

Passing the system tests (CPU test and PCI test) implies that the CPU board is fully operational and can communicate with the rest of the instrument, with peripherals, and with other networked devices.

Frame tests

The frame tests verify the operation of the measurement modules installed in the logic analysis system.

In the 16600A-series, the frame tests verify the operation of the integrated logic analyzer. The frame tests also verify the operation of any measurement module installed in the auxiliary module slot. The slots are designated:

Slot A - Logic Analyzer
Slot B - Auxiliary Measurement Module
Slot 1 - Emulation Module

The installed measurement modules are listed under the selection tabs. Each module can be selected to yield a list of tests available for that module. For more information refer to the service manual of the specific measurement module of interest.

When "Test All" is selected, some of the tests will not run and return a "Not Executed" status because operator action is required. These tests must be selected and run individually by the user. When the tests requiring user action are run, the user is prompted for the specific action that is needed for successful completion of the test. When the indicated user action is performed, and the tested subsystem is operational, the specific test will return a "Passed" status.

For the Agilent Technologies 16610A Emulation Module, the test requiring user action is:

Test:	**User Action:**
Internal PV Test	A loop back connector must be installed

For the existing Agilent Technologies 16500-series measurement modules, the tests requiring user action are:

HP16517A Timing Analyzer Module

Test:	**User Action:**
Skew Adjust	Not a test; used for operational accuracy calibration (de-skew)

HP16522A Stimulus Module

Test:	**User Action:**
Output Stimulus	Not a test; provides continuous signal output Vectors

HP16534A/33A Oscilloscope Module

Test:	**User Action:**
ADC Test	There must be no stimulus on the scope inputs

HP16550A Logic Analyzer Module

Test:	**User Action:**
Show Activity	Not a test; provides continuous output of signal input levels

Passing the Frame Tests implies that the integrated logic analyzer and the optional measurement module are fully operational and can communicate with the rest of the instrument.

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Warning

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock of fire hazard.
- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- If you energize this instrument by an auto transformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the power source.
- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
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- Use caution when exposing or handling the CRT. Handling or replacing the CRT shall be done only by qualified maintenance personnel.

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Hazardous voltage symbol.

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About this edition

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